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# Design and Performance Analysis of Logic Circuits using FinFET Technology

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**ABSTRACT-** As the dimensions of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) decreases, the short channel effect (SCE) becomes a dominating concern in VLSI. The Short channel effect causes an exponential increase in the leakage current. To reduce the SCE and hence leakage current, a new technology has been developed in recent years. In this recent technology a 3D multiple gate MOSFETs like FinFET (Fin Field Effect Transistor) has been developed which possess numerous advantages over conventional MOSFETs and has attracted many engineers anddesigners. FinFET is the new growing technology that works in the nm range to minimize short channel effects. Many companies (like Intel) have started using FinFET technology. This document is a review paper of current research on FinFET technology and discusses how it can be used in future to design new logic devices (like Adder, Comparator, MUX and De-MUX etc.) and memory devices. Various parameters of FinFET like reduced short channel effects, less leakage current, low power consumption, less propagation delay and less time delay are discussed. Various mathematical models and software (HSpice) were used to simulate power, delay, power delay product, average power dissipation and energy delay product. Thus, FinFET technology was designed to eliminatethe problem of SCE by permitting transistors to be scaled down into sub 20nm range.

**KEYWORDS-** FinFET, MOSFET, GDI, Shortchannel Effects, Power Consumption, Power- Delay Product.

## I. INTRODUCTION

As nanometer process technologies haveadvanced, chip density and operating frequency have increased, making power utilization indevices a crucial issue. So, for the designers ofVLSI (Very Large-Scale Integration) the main goal is to fulfill performance requirementswithin a power requirement. Hence there is an increased importance of power efficiency.

In FinFET technology, which is an emerging technology, offering interesting power delay trade-offs, is likely to augment CMOS (Complementary metal Oxide semiconductor) when scaled down to 32nm and beyond.

In design metrics, we have performance, area, cost, and time to open-air market. Since the beginning of the Integrated Circuit industry, thedesire to optimize this design metrics has not changed. Moore's law, in fact, is all about optimizing these parameters. However, as scaling continued, and the manufacturing nodesprogressed towards 20nm, some parameters especially the power supply voltage, which is the main factor in determining the dynamicpower could not be scaled any further. One more issue was optimizing in one variable demands in big compromises in other variables,for example, performance optimization caused degradation in power factor.

Hence the design window was shrinking for optimizing among the design variables. ButFinFET broadens the design window once again.Dynamic and static power was saved significantly as operating voltage continues scaling down. Short cannel effects are reduced significantly. Hence continuing to improve performance compared to planar device at an identical node. Performance advantages of the FinFET widen compared to its planar equivalent, because of superior gate control of the channelin FinFET.

As compared to budget are counterpart, one major design optimization benefit of FinFET is the factthat it gives much higher performance at the very same power budget, or at a much minimum power budget it provides equal performance. Hence giving the designers and engineers the potential to extract the higherperformance for the minimum power, which is a much-needed requirement for devices which operate on batteries.

In VLSI, thousands of circuits based on transistors are connected and combined to create integrated circuits (IC's). One example of VLSI device is a microprocessor. In the current era, VLSI architectures are used in the manufacturing of almost each and every chip today.

To meet these demands size, efficiency andpower must be reduced. For the design of both analog and dialog circuits, power dissipation is the most important objective to be optimized. By using the FinFET technology as compared to the circuits implemented in CMOS, the average leakage power, the clock power, and the total active mode power consumption are reduced up to 53%, 29%, and 55% respectively for the combinational circuits, while maintaining similar data stability and speed.

## II. LITERATURE REVIEW

Some of the literature pertaining to design and performance of Logic circuits using FinFET technology is discussed as follows:

**Debajit Bhattacharya et al.** [1], has proposed the various types of FinFET based devices and designed them into their structures. They also discussed the sources of process fluctuations in FinFETs and their effect on FinFET

performance. They describe FinFET inverter and NAND gates, DRAM, SRAM latches, and flip flop cells. In their research paper they discussed circuit level analysis and optimization methodologies and then presented a survey of process-voltage- temperature (PVT) variation aware architecture-level simulation tools.
They look over techniques for making Fin-FETdevices and circuits distinctive and look at FinFET based logic gates, memory cells, and flip flops. They mention leakage-delay tradeoffs that are achievable at each level of the design hierarchy.

**Aqilah binti Abdul Tahrim** et al.[2] worked on Design and Performance Analysis of 1-Bit FinFET Full Adder Cells for Sub threshold Region at 16 nm Process Technology. 1Bit FinFET based full adder cells were designed forSub threshold region at 16 nanometer process technology. It is necessary that we have an efficient & reliable adder consuming less powerand possessing enough speed. Compared to typical Complementary Metal Oxide Semiconductor technology, they implemented FinFET technology in 1bit full adder cells, to extend Si downsizing and improve the performance and energy efficiency of Full Adder. They have discussed 4 types of cells designs they used in FinFET based full adder, which are CMOS, Complementary Pass- Transistor Logic, Hybrid CMOS, and Transmission Gate. They used HSPICE for circuit development and simulation. They used PTM CMOS technology & BSIM CMG Models for FinFET based technology to adapt design libraries. They analyzed the average power dissipation, propagation delay, energy-delay product and power-delay-product based on all 4 cell designs. In 2006 ITRS gave an account of a matter on the scaling process of MOSFET to 32 nm. This issue highlighted thatscaling planar bulk CMOS into a compact size faced a lot of problems because of the huge doping that was required, and trouble in adequately controlling SCE. However, the issueof scaling CMOS into the nanometer region was solved by putting new structures into practice such as FinFET.

**M. Vamsi Prasad et al.** [4] discussed theeffect of short channel effects (SCE) that give rise to rapid increase in the leakage current. Tominimize the SCE, FinFET technology is used. FinFET technology is the latest emerging technology that can make transistors work in the nanometer range to overcome SCE. They also implemented a low power FinFET based Full Adder by using CADENCE VIRTUOSO tools in 45nm technology with the supply voltage of about 1V in CMOS and 15nm technology with the supply voltage ofapproximately 0.7V in FinFET. They alsoanalyzed delay, power, and power- delay product for FinFET based Adder. The results show that the PDP of GDI FinFET Full Adder is reduced to 66% compared to FinFET Full Adder.

**Himani Singh Rana et al.** [5], has proposed the key features and challenges associated with FINFET and the comparison of FinFET with CMOS. Subsequent discussions reviewed some of the unique features of FinFET, which result in behavior different from simplicity of MOS transistors.
Their research paper gives a comparison ofFinFET with CMOS, so FinFET inverter and CMOS inverter values are taken to resolve the problem of average power, maximum power, delay, and power dissipation.
This paper also shows that FinFET technology is far better than CMOS technology. FinFET operates at a minimum voltage because of their low threshold voltage and the leakage current isreduced by about 89%. FinFET technology has authorized the development in Integrated Circuit technology to continue to obey Moore'slaw.

**Sneha Arora et al.** [7] has proposed a technique for performance improvement and noise tolerance in dynamic logic circuits. Using FinFET technology, they have designed an AND gate with two inputs and simulated it in 32nm technology. Simulation results show that the proposed technique comes up with refinement in noise tolerance of about three times & the useof FinFET device minimizes the expenditure ofpower than the MOSFET designs.

**Bibin Lawrence R Jency Rubia J** [8] worked on FinFET Technology and Circuit Design Challenges. In their research they have discussed FinFET technology and the circuit designs using FinFET technology. Their work gives a clear picture of both advantages and disadvantages of FinFET. This paper gives the key features and challenges associated with FINFET. Considerable changes have been put forward to circuit design by FinFET. There are yet various challenges and constraints that FinFET technology must face to be more successful than other technologies: fin shape, doping, isolation, stressing, pitch & crystallographic orientation as well as device performance was discussed.

**M. Pavan Kumar et al.** [9] has proposed an efficient full adder using FinFET Technology. They make survey on Adder type of devices which gave you addition, subtraction and all arithmetical operators performed in circuit leveland logic level implementation. And they designed new technology named FinFET basedadder circuits which give better performance like less Leakage power, reduced propagation delay and less power consumption. They also verified all the parameters in 45nm Technology node to both CMOS and FinFET technology by using Hspice software.
As per survey, they consider MOS transistors- based propagation delay, average power, and product of those two factors. Hence observed Gate Diffusion input (GDI) based Full adder consists of less power consumption, less area delay, and a smaller number of transistors. After that they went for FinFET based full adder system in normal 28 transistors and GDI based FinFET system have very less powerconsumption at 45nm technology node and lessdelay in the system. Hence, they concluded that FinFET based Adder system has better power consumption and less delay in the circuit.

**Harshita Gehlot et al.** [10] studied theanalysis of Proposed FinFET Based Full Adderusing CMOS Logic. To enhance the architecture of Full Adder various improvements have been made. So, to minimizethe Short Channel Effects (SCE), they haveproposed a FinFET based Full Adder.

**Rachana A Patel et al.** [15] formulated a document which gives a review of current research trends in FinFET technology and discussed its capability to change the future of nano-scale electronics. Various parametric advantages as well as issues with FinFET technology were discussed. They presented Physics level design requirements for FinFET device modeling and logic design approaches. Various mathematical models used to simulate the FinFET devices were reviewed. Recent replacement of planar MOSFET with FinFET in primary circuits of a complex design is also discussed.

**D. J. Frank et al.** [16] discussed about Device Scaling Limits of MOSFETs and their application dependencies, most of the important physical phenomenon that is short channel effect, powerconsumption and leakage current that comes inthe way of continuous scaling of Metal Oxide FET technology & have shown how the above- mentioned effects place a limit for different circuit applications. They have presented scale length theory which provides a useful framework to grasp the tradeoff betweenchannel length and SCE.

They have also shown that for high performance logic CMOS should be scaled down to about 14 nm and to 35 nm for very lowpower applications.

Overall, they concluded that scaling of CMOS does not have any end point. However, there are several end points, each modified to its function.

**Richa Saraswatal et al.** [17] worked on Optimized Complementary Metal Oxide Semiconductor (CMOS) design of Full Adder using 45nm Technology. This paper provides the design of a low power full adder using 45 nm technology which reduced the area, power,and delay. They compared 28T CMOS full adder using 45 nanometer technology with 8T and 16T full adder in terms of power, delay, andarea. To create layout of all the three designs, they used micro-wind tool. In their result they showed that 8T full adder consumes nearly 97%less power than 28T and 66% less power than 16T full adder.

**Prasad M et al**. [19] worked on Comparative Study of 1Bit Full Adder cells using FinFET, implemented using CMOS & TG logic a 32nm, 22nm, and 10nm. Using two logicstyles they did comparative analysis of differentfull adder cells. They used CMOS & TG logic for implementing 1Bit full adder. They have done simulations of full adders at a scale of 32,

20 & 10nm. For simulations of multi-gate transistors, they make use of PTM models. Thecharacteristics that were measured, compared, and examined are leakage power, average power, energy, and delay. It was also observedthat Transmission Gate based full adder consumes less power than conventional CMOSfull adder in 10nm.

**R. A. Thakker et al**. [20] proposed a process technology ofFinFET and the comparative study of MOS, CMOS and FinFET technologies. It has been shown that conventional CMOS on scaling beyond 32nm, FinFET technology becomes a better alternative for it and shows high performance for low power applications. It has been shown that FinFETs have achieved many ways to minimize leakagecurrent, dynamics current, short channel effect and delay over conventional CMOS and MOSFET. Thus, FinFET is a better alternative totackle SCEs below 32nm node.

**Problem Statement**: Metal Oxide Semiconductor Field effect transistor (MOSFET) has been commonly used in current technology. After 32nm technology it becomes difficult for the Gate to control the channel of the MOSFET and thus cannot turn off the channel completely.

**Proposed Research Work**: Increasing the gate- channel capacitance reduces this drawback. Hence to design devices below 32nm a new technology has been proposed, the so-called multi-gate transistors, like FinFET stands out.

Thus, the objective is to design and study performance analysis of logic and memory circuits using both MOSFET and FinFET. Doingcomparative analysis of circuits using MOSFET and FinFET in terms of time delay & power dissipation.

## III. METHODOLOGY

To increase the speed and performance of integrated circuits many ways have been tried by the researchers. Due to which the number oftransistors per integrated circuit or chip get increased by two times every year following thewell-known Moore's law. This rise in the of transistors count has been achieved either by increasing the chip's size or by minimizing the transistor size. However, minimizing the transistor size is the main reason for increased chip density. We have seen that as device size is scaled downto 28nm, researchers face lot of barriers relatedto its fabrication and characteristics. At that small dimension transistor performance isaffected by short channel effects. The Short channel effect causes an exponential increase inthe leakage current between the source anddrain terminal even when the device is off,causing the gate to lose control over channel to such an extent that it cannot turn off the channelcompletely. This and other technical challengesdrove researchers to go for alternative transistordesigns.

Thus, FinFET technology was designed to eliminate the problem of SCE by permitting transistors to be scaled down into sub 20nm range.

As the dimensions of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) decrease, the short channel effect (SCE) becomes a dominating concern and leads to increase in leakage current and thus power dissipation increases. To reduce leakage current, hence power dissipation a new technology, known as FinFET technology has been proposed to design logical devices. Different devices like Inverter, Adder and MUX etc. have been designed using both CMOS and FinFET technology to compare various parameters like power dissipation,

delay, and power delay product. Here in this research, we have tried to design these circuits at channel length of 16nm using spice software. So, this paper compares FinFET technology withCMOS technology.

DESIGN of Logic and Memory Circuits:

First, we designed all the circuits using CMOStechnology at 16nm channel length and thevalues of different parameters have beencalculated as mentioned in table 1. Also, we used the PTM model in design and simulation of all the circuits.

Again, using FinFET technology all the above circuits at 16nm channel length have been designed. After designing, the Voltage transientcharacteristics have been obtained for each circuit using Spice Simulator tool. And different parameters like power dissipation, time delay and power delay product have been calculated as shown in table 1,2,3 respectively.The output waveforms of all the above designed gates and circuits are shown in figures. All the figures show the input and output waveforms generated from the HSPICE simulation. The output of all the devices produced is as expectedin the truth table as tabulated in Table.

### *A. Design of Inverter*

This is the most basic gate, with one input and one output. It produces a '1' output if the inputis '0' and vice-versa. That is, it produces an inverted version of the input at its output. That is why it is also known as Inverter.

The design of CMOS inverter is shown in figure 1

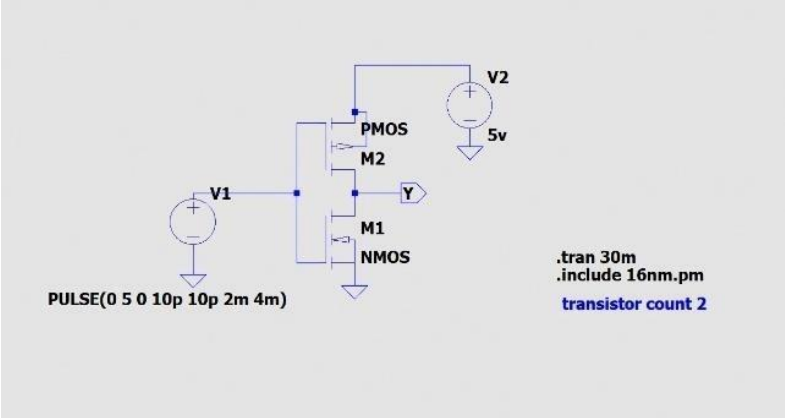



Figure 1: Inverter using CMOS logic

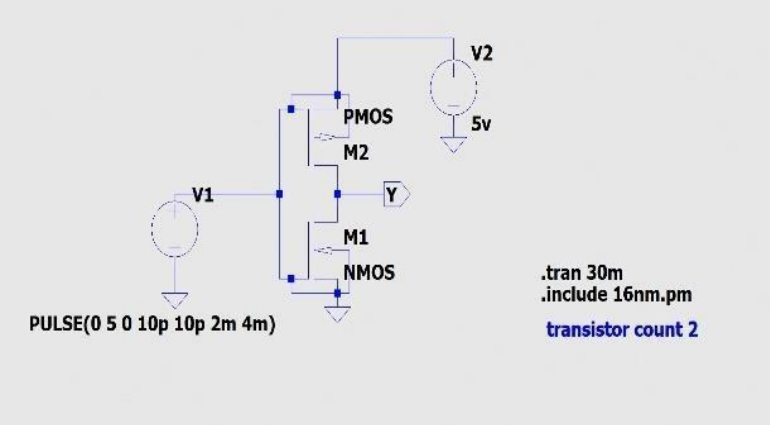



Figure 2: Inverter using FinFET technology

We used HSPICE software, for design of inverter of 16nm channel length and then simulated the circuit using PTM model.

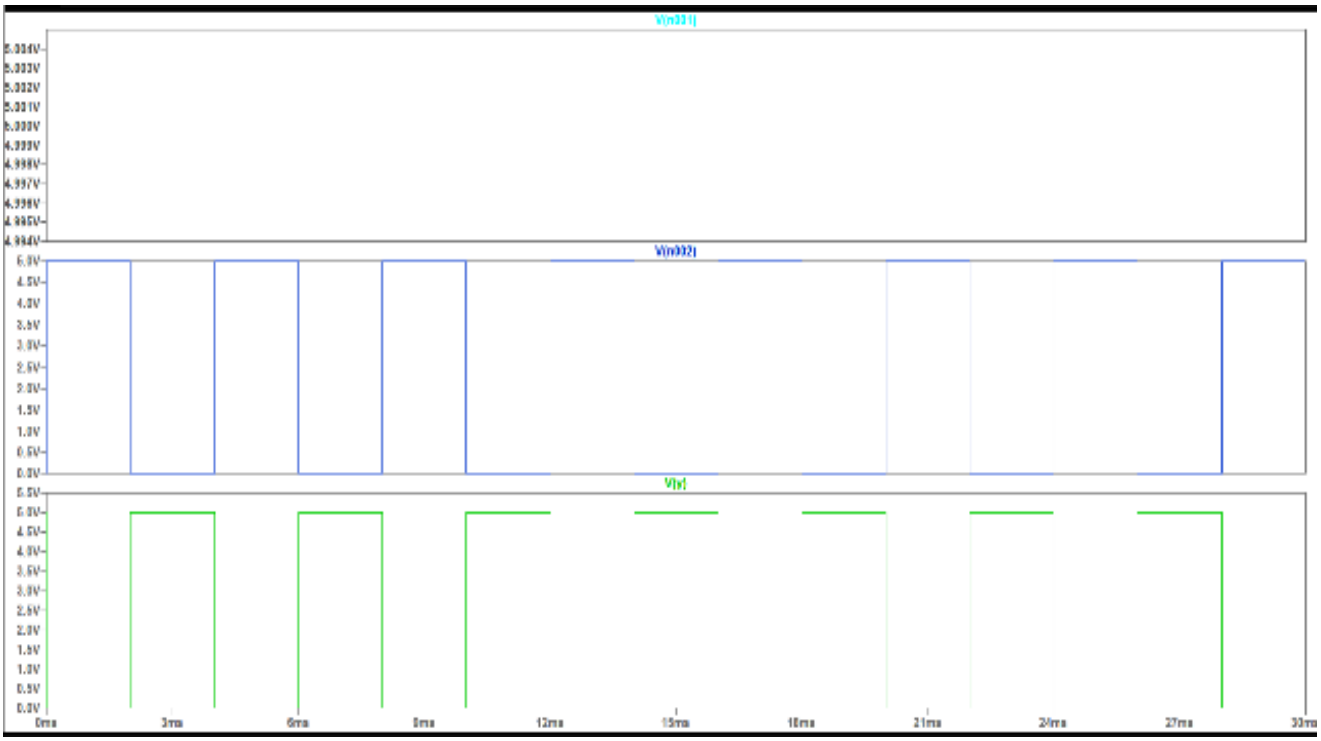


Figure 3: Output waveform of Inverter

### *B. Design of NAND*

This is an AND gate followed by NOT gate. The gate gets its name from NOT AND behavior. NAND gate is also called universal gate since by using these gates you can realizeother logic gates like OR, AND & NOT. If both the inputs are '1', the output is not '1'.

The design of NAND gate is shown in figure 4.

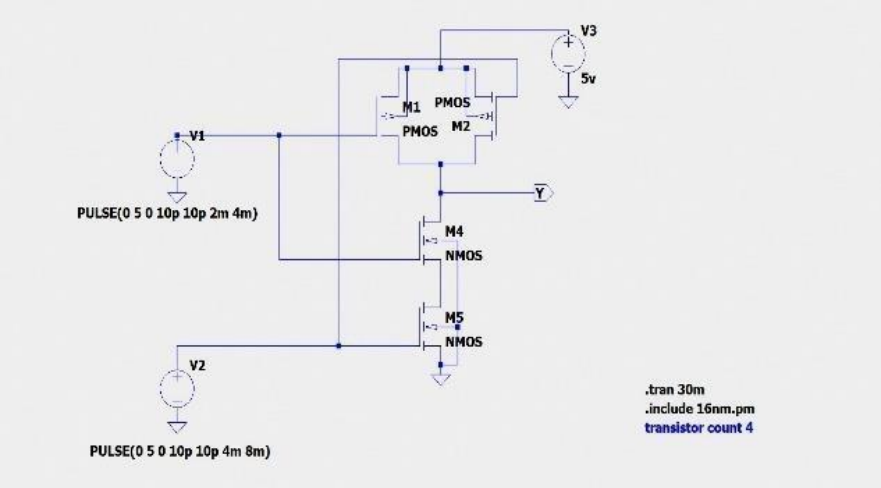



Figure 4: NAND gate using CMOS logic

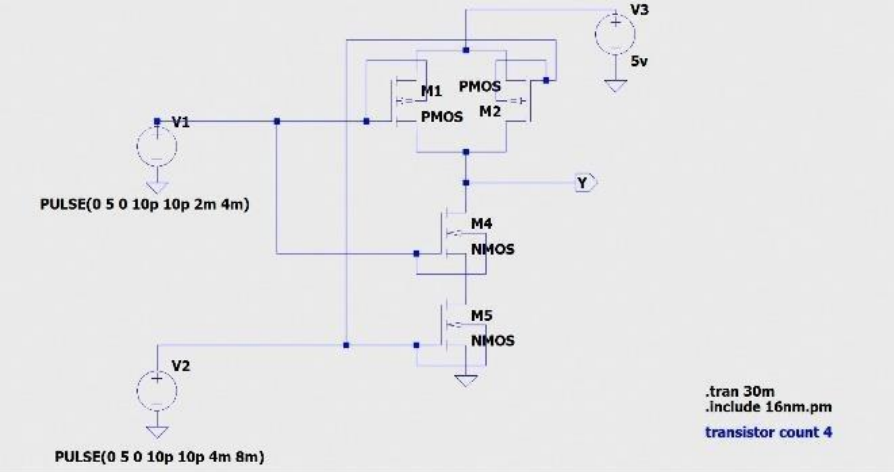



Figure 5: NAND gate using FinFET technology

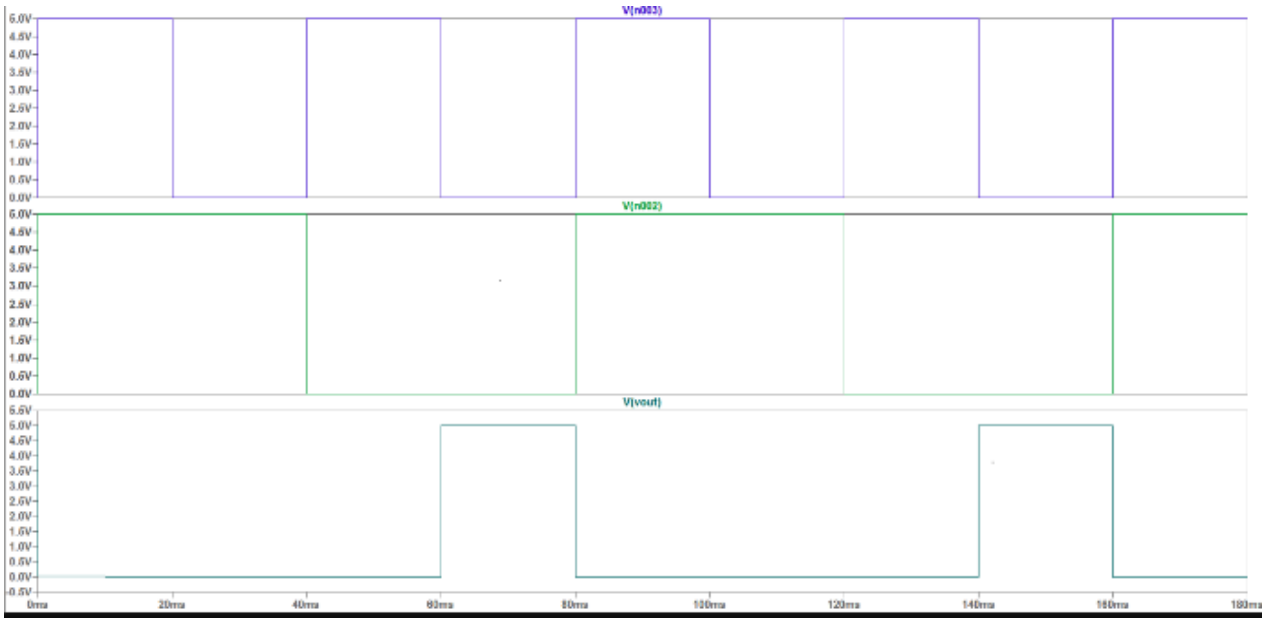



Figure 6: Waveform of NAND gate

### *C. Design of NOR*

It has two or more inputs and one output. A NOR operation applied after, or gate gives a NOT-OR gate. Its output is '1' only when boththe inputs are '0.'
The design of NOR gate is shown in figure 7.

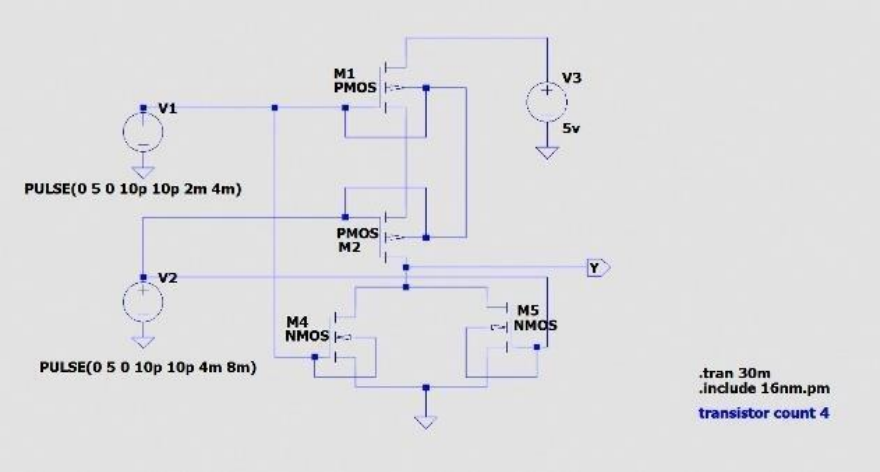



Figure 7: NOR gate using CMOS

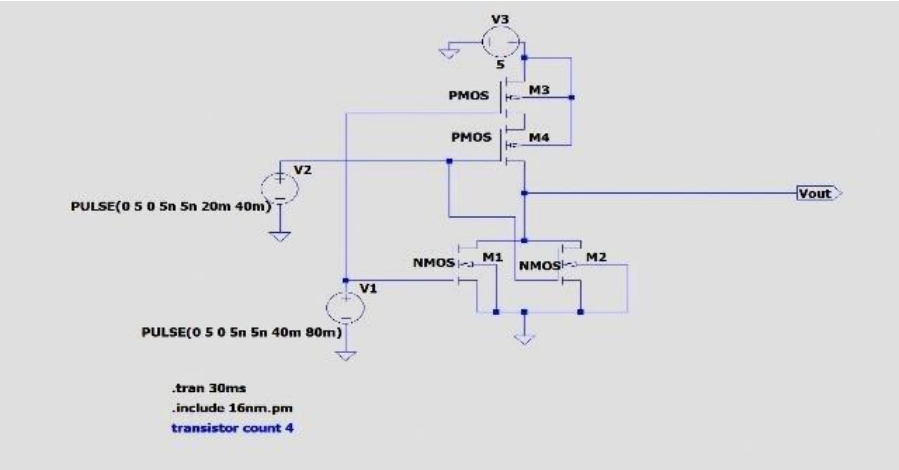



Figure 8: NOR gate using FinFET technology

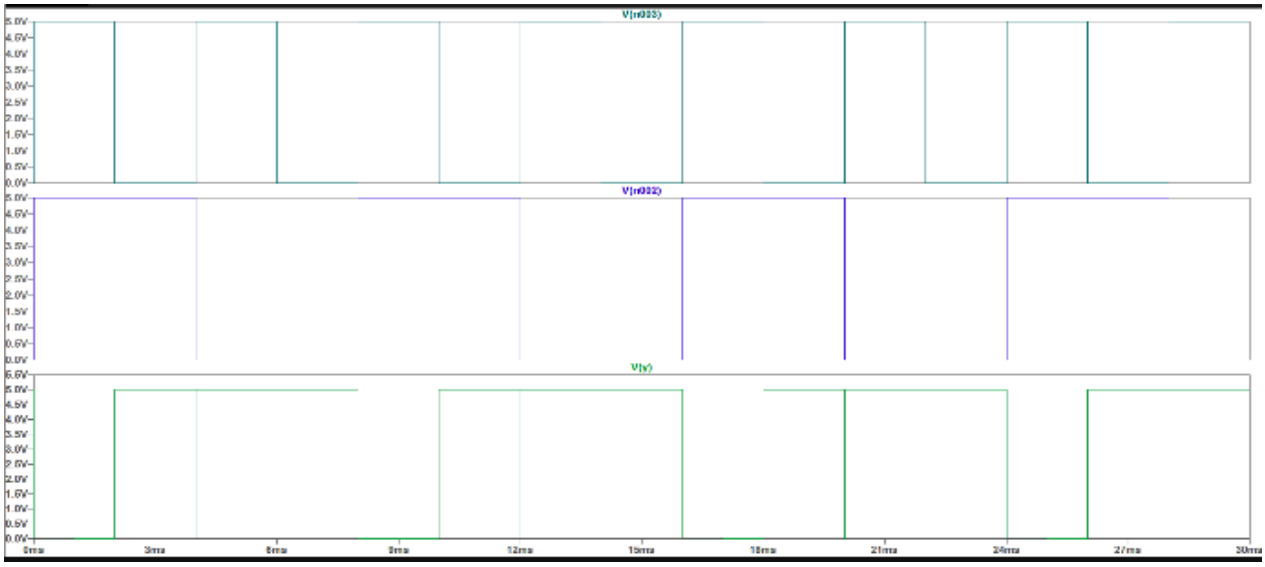


Figure 9: Output waveform of NOR gate

### *D. Design of Half Adder*

It is a combinational circuit and performsaddition of two binary numbers and gives Sum & Carry as output. Its Truth Table and gate level representation is given below.

The value of Sum ranges from 0 to 2 in decimalfor addition of two bits. So, we need two bits for representing it in binary system.

The design of Half Adder is shown in figure 10.

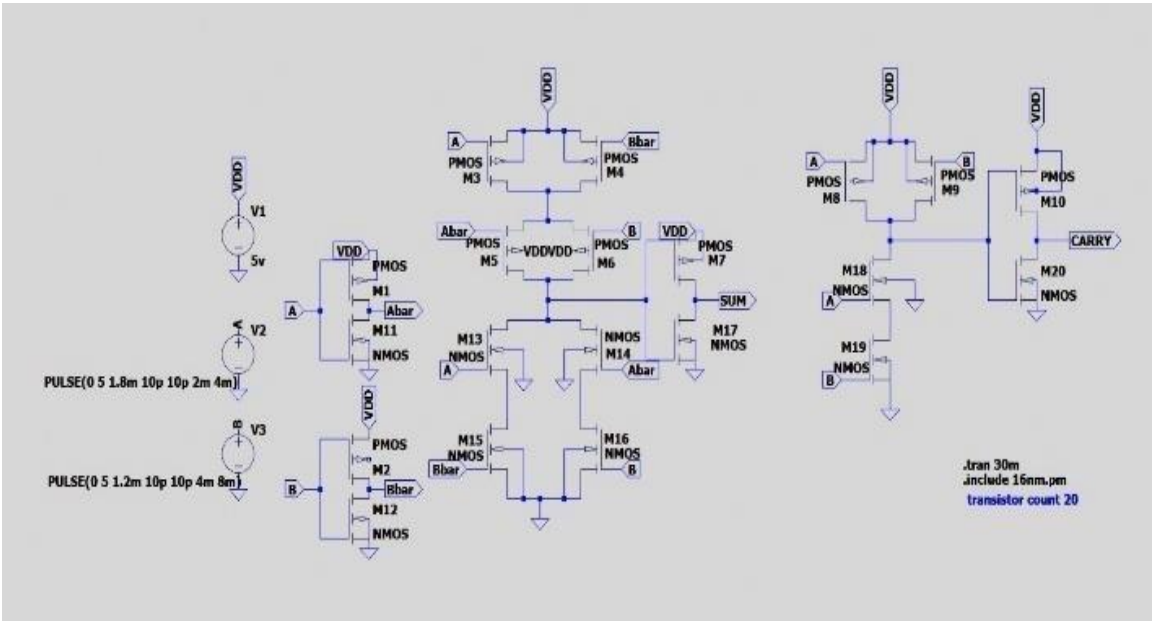



Figure 10: Half Adder using CMOS logic

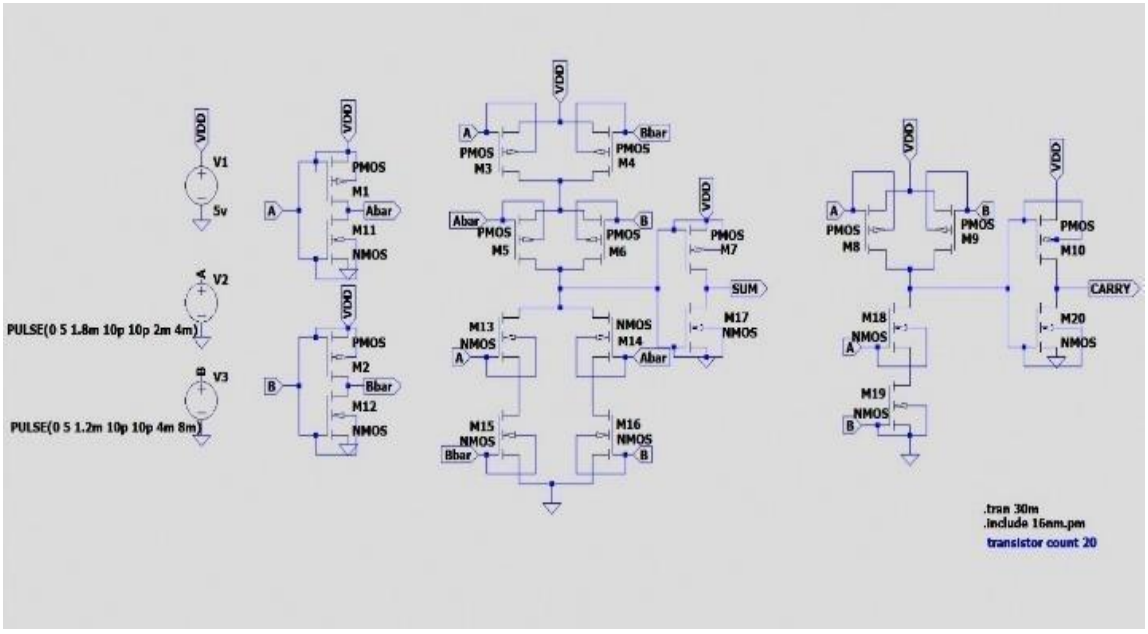



Figure 11: Half Adder using FinFET technology

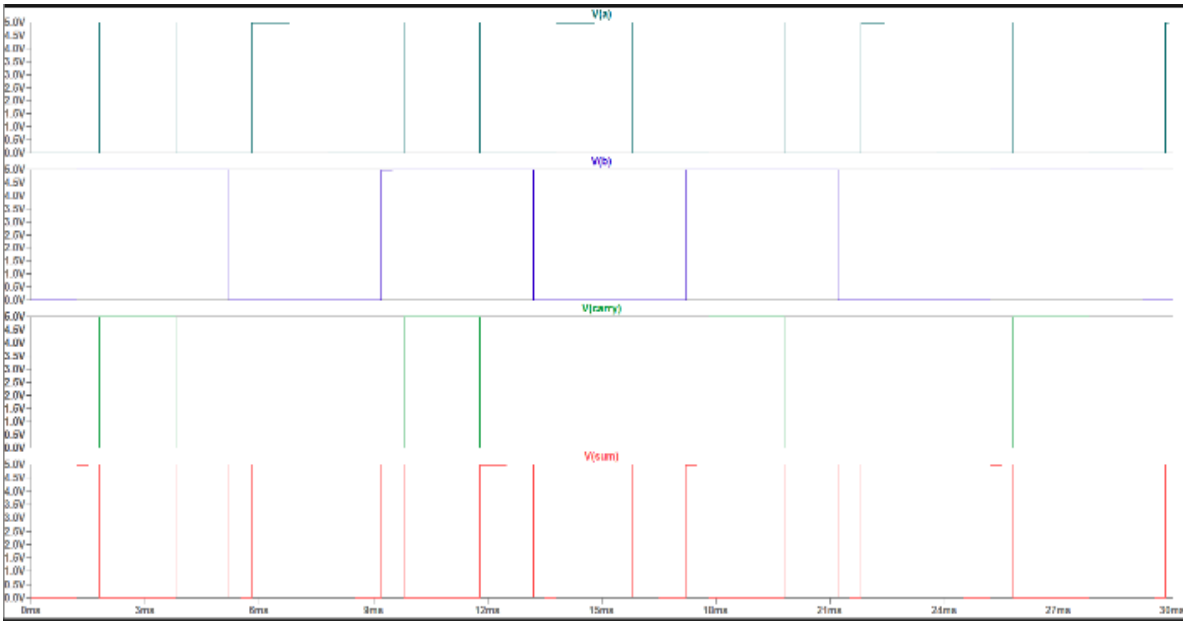



Figure 12: Waveform of Half Adder

### *E. Design of Full Adder*

It is a combinational circuit and performs addition of three binary numbers and gives Sum and Carry as output. The expression for Sum and COUT is given by:

$$C_{out} = A \cdot B + Cin \cdot (A \oplus B)$$

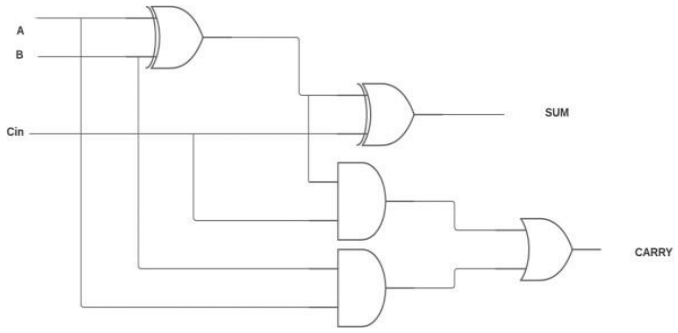
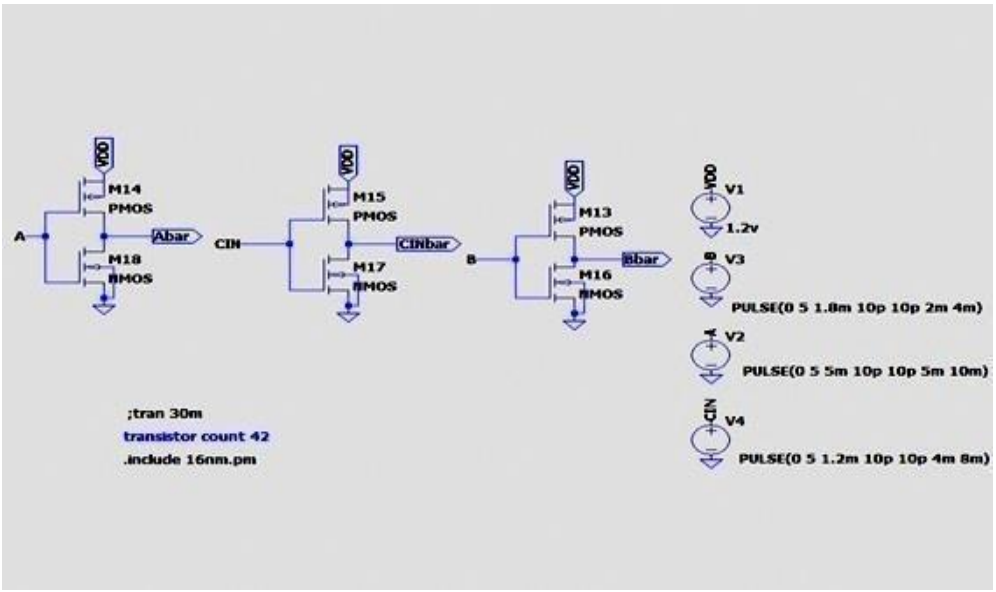
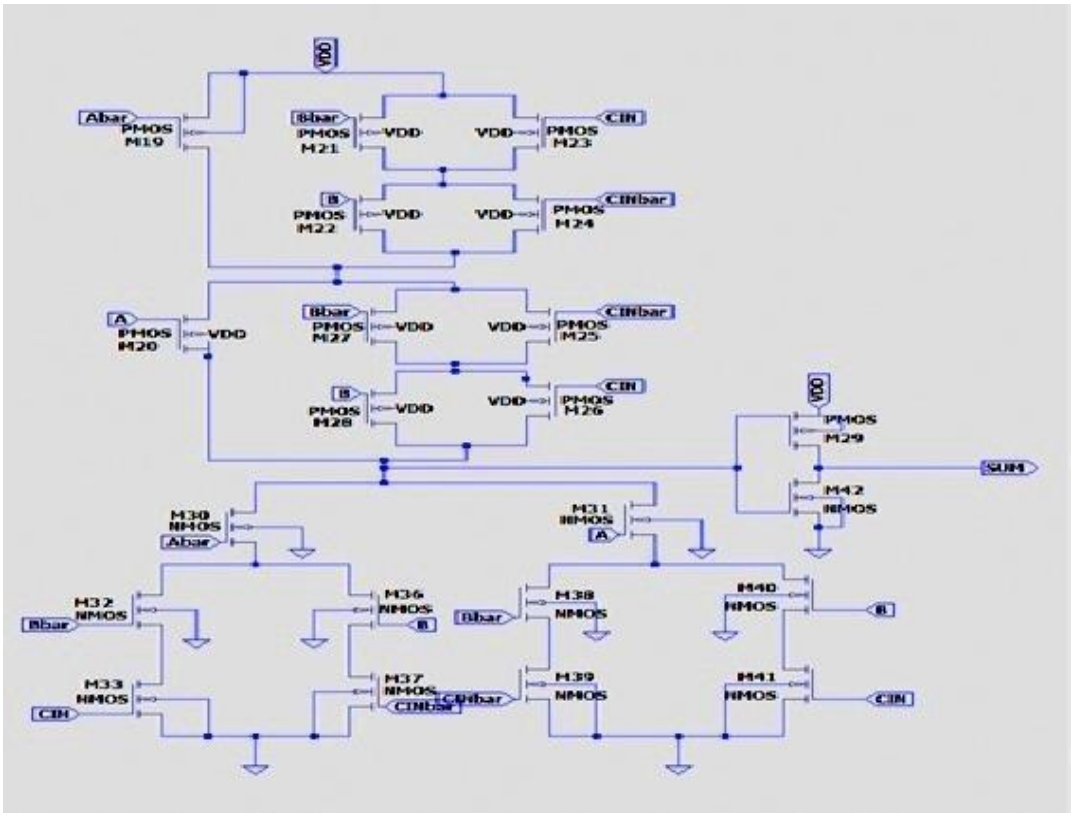



Figure 13: Full Adder using logic gates

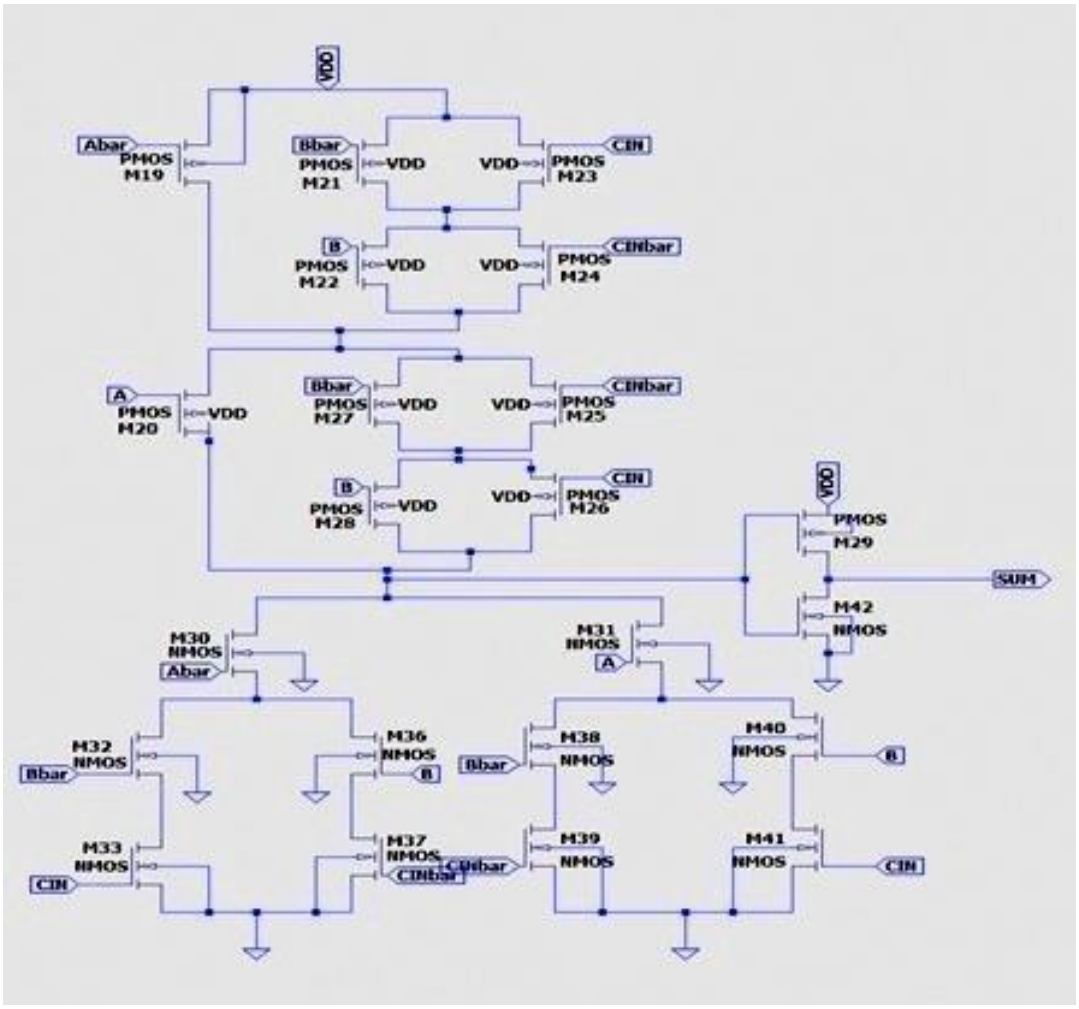
The design of Full Adder is shown in figure 14.




(a)




(b)




(c)

Figure 14 (a), (b), (c) represents Full Adder using CMOS logic

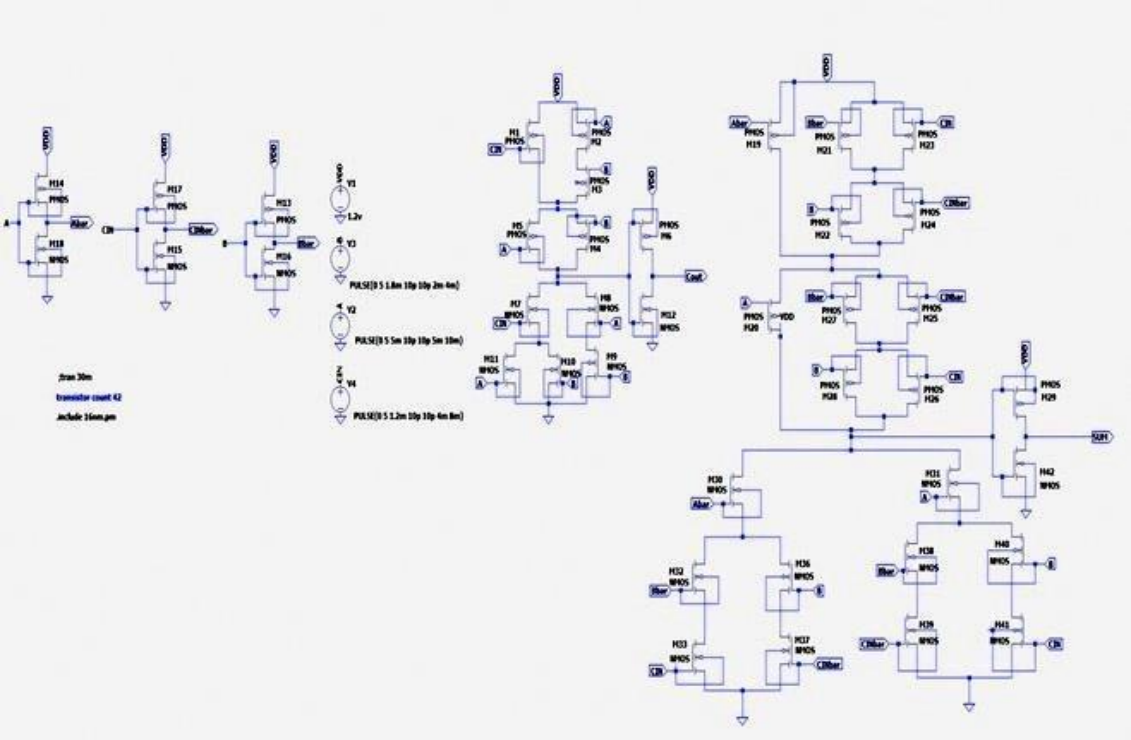


Figure 15: Full Adder using FinFET technology

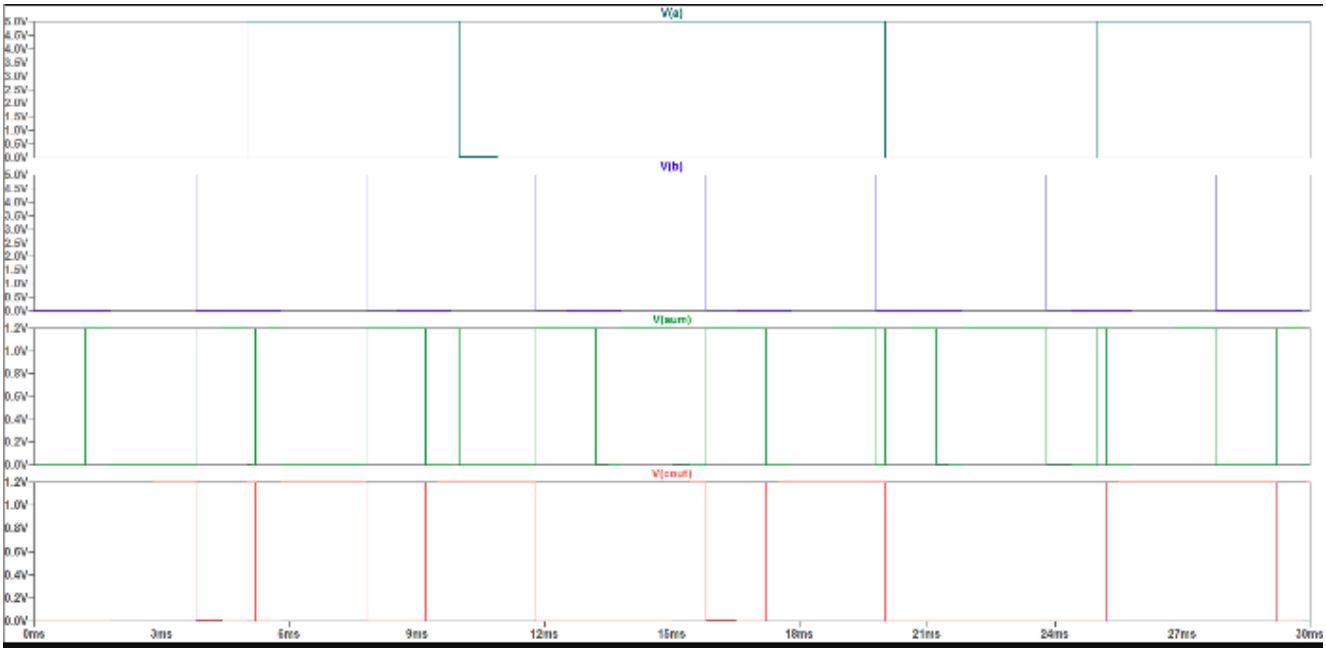



Figure16: Waveform of Full Adder

### *F. Design of 2:1 MUX*

Multiplexer, also known as data selector, is a device that selects between several analog or digital signals and forwards the selected input to a single output line. The selection is directedby a separate set of digital inputs known as select lines, say S1 and S2.

A multiplexer of 2n inputs has n select lines, which are used to select which input line to sendto the output. Multiplexer can be of different types depending on number of inputs like 2:1 MUX ,4:1 MUX. Etc. but, in our research, we have worked upon 2:1 MUX. The block diagram of 2:1 MUX is shown in figure. I0 and I1 are the two inputs and S0 is the select line which selects among I0 and I1 and send to the output 'f'. The design of 2:1 MUX using logic gates is shown in figure 18.

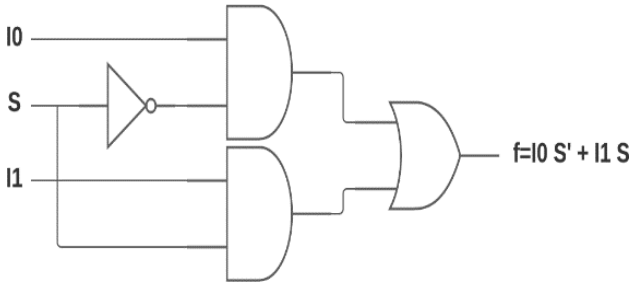



Figure 17: 2:1 MUX using logic gates

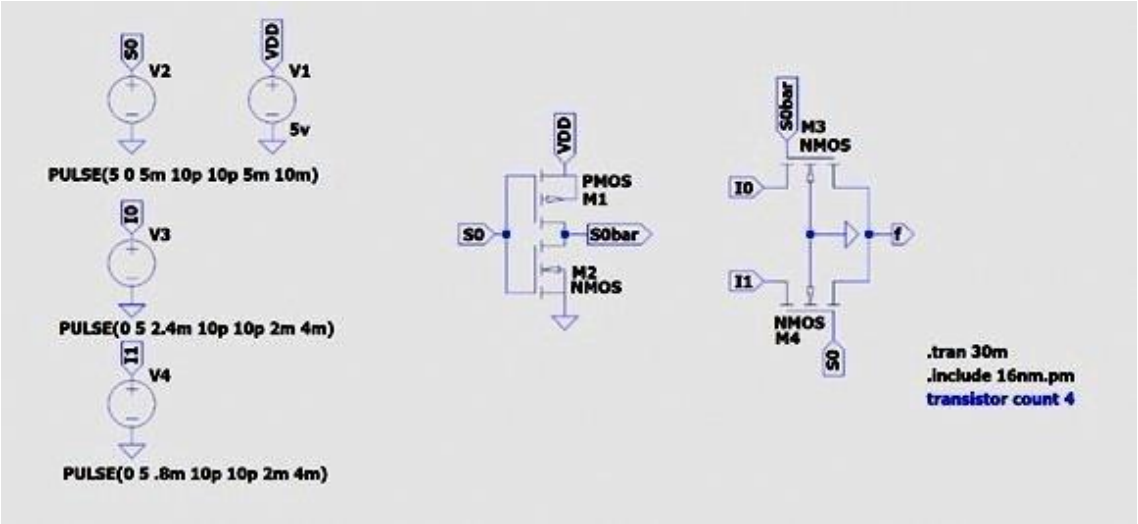



Figure 18: 2:1 MUX using CMOS logic

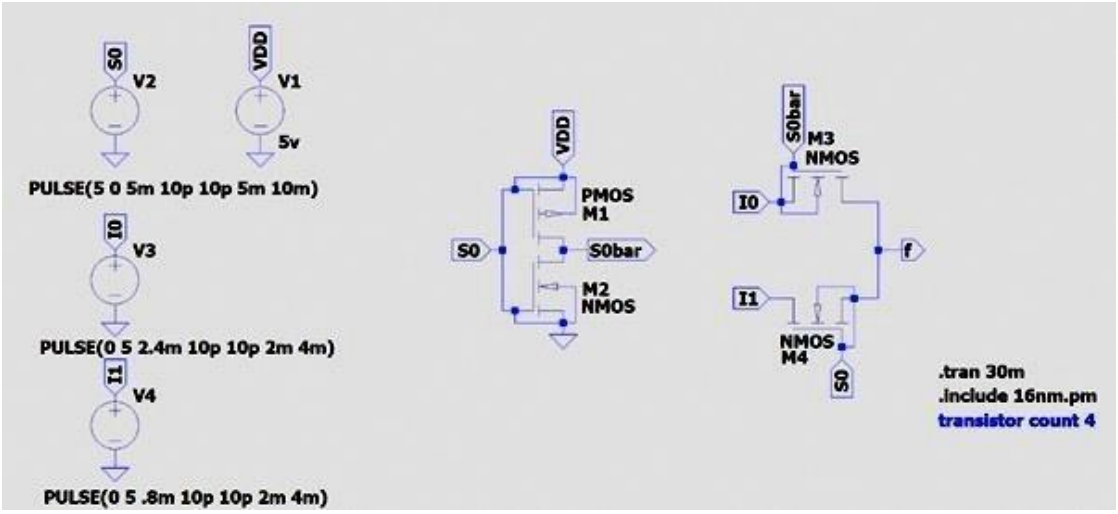



Figure 19: 2:1 MUX using FinFET technology

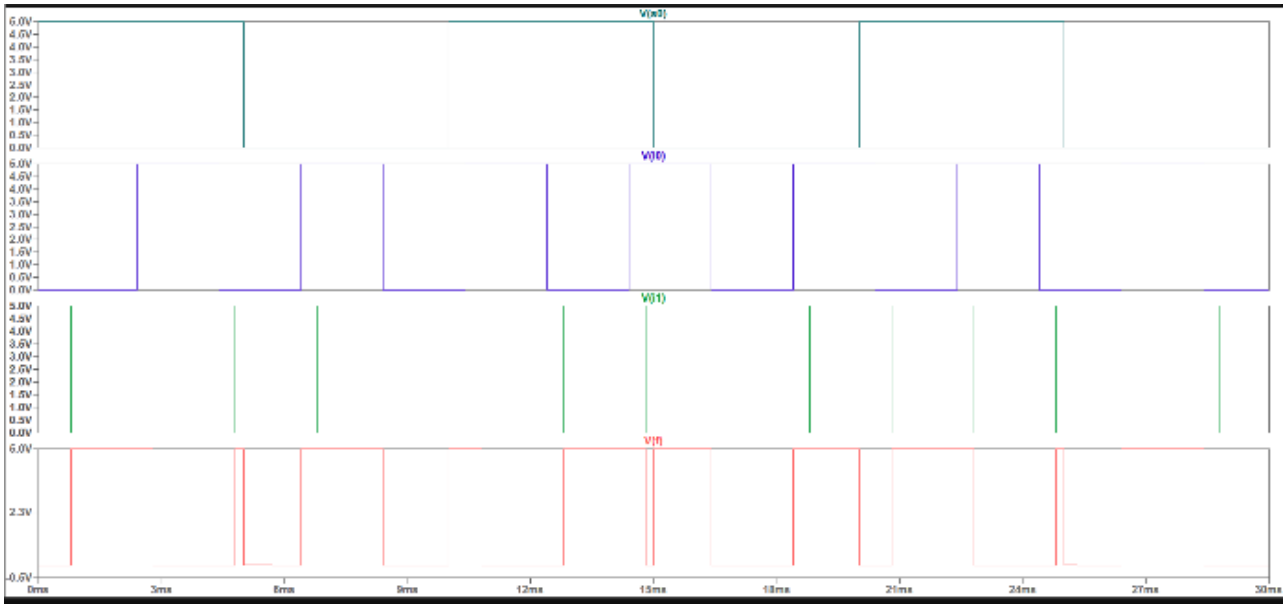


Figure 20: Waveform of 2:1 MUX

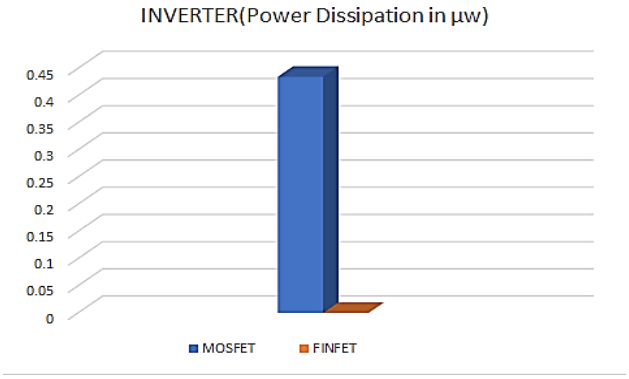
## IV. RESULTS AND DISCUSSION

Table 1: Power Dissipation comparison between MOSFET and FinFET

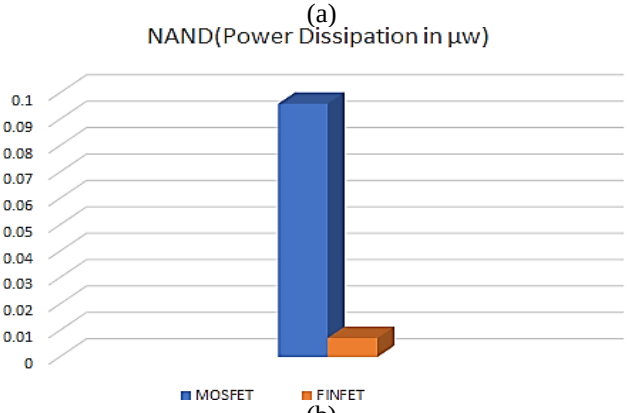
| DEVICE | MOSFET | FINFET |
|---|---|---|
| INVERTER | 1.989µ | 1.697µ |
| NAND | 1.891µ | 1.254µ |
| NOR | 1.781µ | 1.321µ |
| Half Adder | 2.001µ | 1.892µ |
| Full Adder | 3.750µ | 2.675µ |
| 2:1 MUX | 2.654µ | 1.321µ |

The figures 3,6,9,12,16 and 20 depict the variation of output voltage with respect to timewhich help us to find out average power dissipation and time delay at 16nm channel length, maintaining the same power supply as mentioned in table 1 & 2.

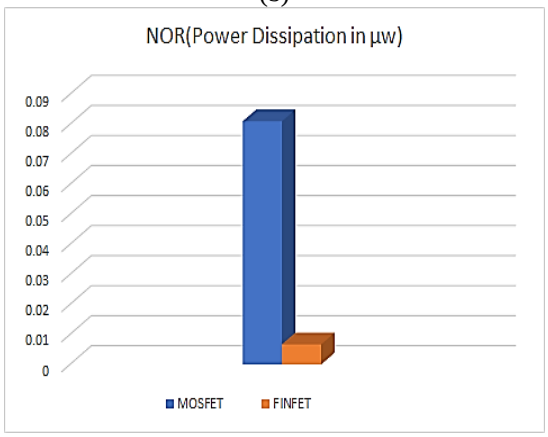
Following graphs gives clear view of the powerdissipation and time delay comparison between MOSFET and FinFET based circuits. Here we can clearly relate the power dissipation andtime delay in each circuit based on both CMOSand FinFET technology. Power dissipation ismore in COMOS based circuits than FinFET based circuits, so CMOS based circuits consume more power as compared to FinFET circuits. Also, time delay calculated in microseconds is more in CMOS circuits than FinFET circuits. First six figures depict relation of power dissipation in each circuit designed using both CMOS and FinFET technology and the last six figures shows time delay of each circuit designed using both the technologies.



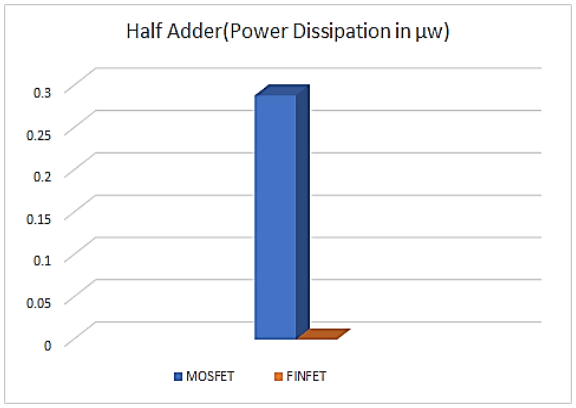

(a)



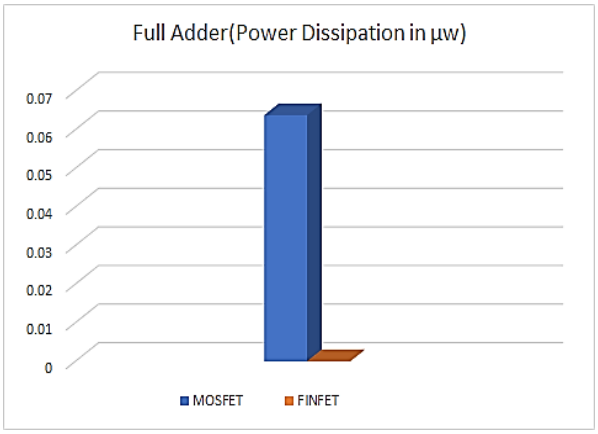

(b)



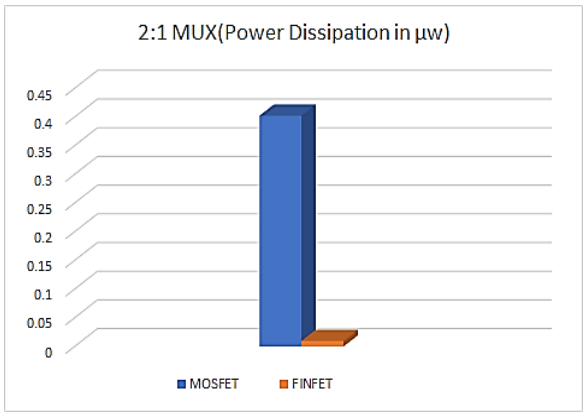

(c)




(d)




(e)

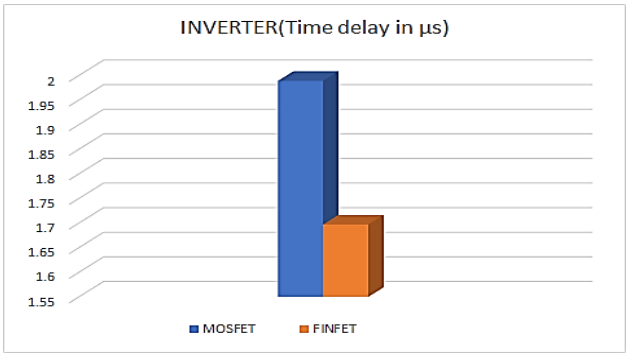



(f)

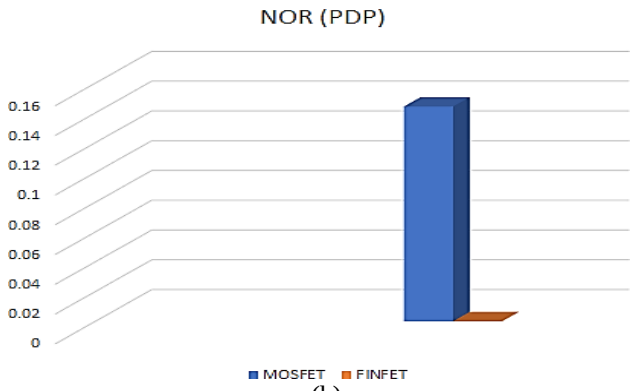
Figure 21: Power Dissipation of (a) Inverter, (b) NAND gate, (c) NOR gate, (d) Half Adder, (e) full Adder, (f) 2:1 MUX.

Table 2: Time Delay comparison between MOSFET and FinFET

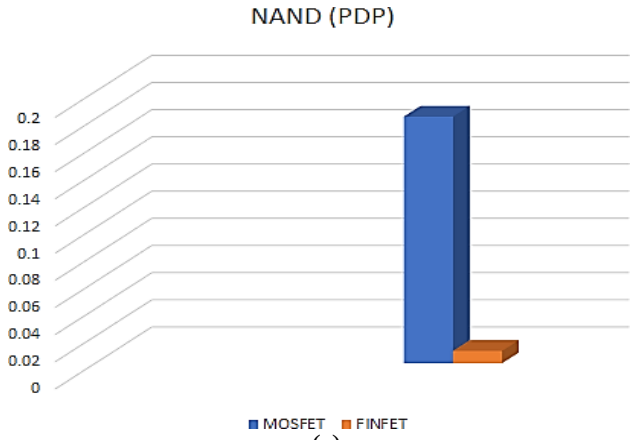
| DEVICE | MOSFET TECHNOLOGY | FinFet Technology |
|---|---|---|
| INVERTER | 434.426n | 527.4346f |
| NAND | 0.096µ | 0.0072µ |
| NOR | 0.081µ | 0.0067µ |
| Half Adder | 0.28873µ | 126.6p |
| Full Adder | 0.0638µ | 85.1236p |
| 2:1 MUX | 402.35n | 9.7n |



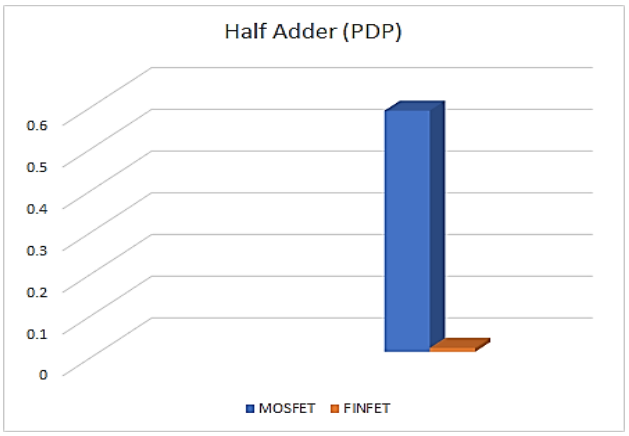

(a)



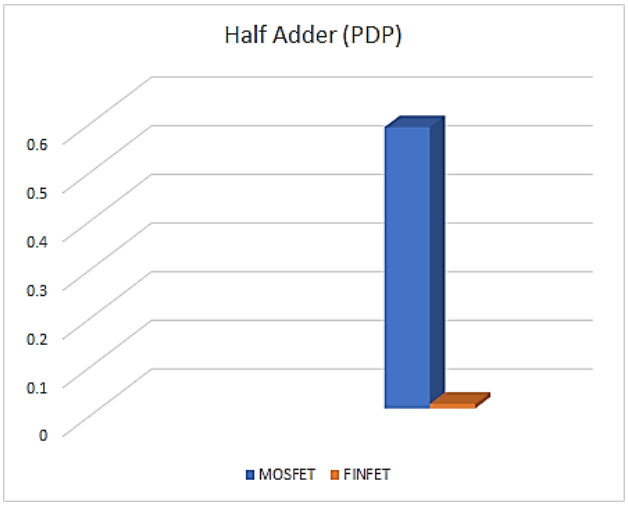

(b)



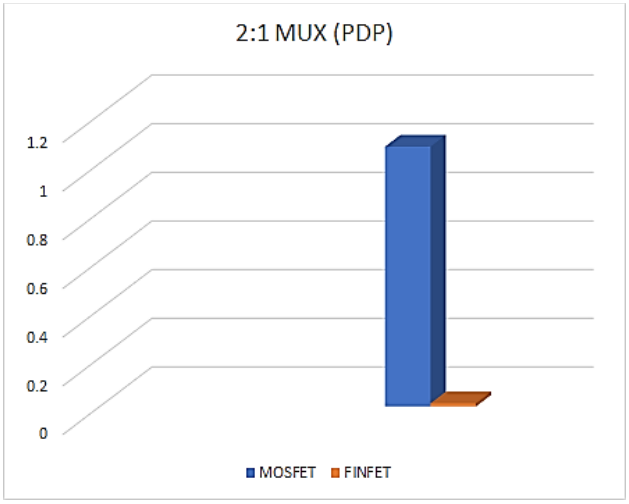

(c)




(d)




(e)




(f)

Figure 22: Power Delay Product of (a) Inverter, (b) NAND gate, (c) NOR gate, (d) Half Adder, (e) full Adder, (f) 2:1 MUX.

## V. CONCLUSION AND FUTURE WORK

As we have seen in this thesis work, FinFETs offer far superior results as compared to the conventional MOSFETs. The power dissipation and time delays occurring due to the circuits based on FinFETs has been drastically lowered. Power consumption and time delays are among the most important parameters in checking the performance of a digital circuit, especially in those devices which are portable and require batteries to operate.

As per the designs space offered by the FinFET devices, it is very much possible that FinFET devices will replace the conventional transistorsunder the technology node of 16nm and beyond.

Due to their ease of fabrication process, and much better performance, FinFET is emerging asa very good option in replacing the conventional transistors. As compared to the conventional transistors, the fabrication processof FinFETs is almost similar.

Intel has already announced the tri-gate FinFET as its choice, at the technology node of 7nm forthe manufacturing of its processors.

In this research work digital arithmetic circuitsare built using the short gate type of FinFET devices. The other type of FinFET device i.e., independent gate also gives diverse design options, because in it, we can independently control the two gates and control the channel more efficiently leading to more innovative ways of design, but at the cost of more area, dueto the requirement of two connections of the front and back gates.

## CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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