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A Novel Multilevel Converter with Stable Voltage to The Renewable Energy Systems

Vathala Nagi Reddy
UG Student, Department of Electrical and Electronics Engineering in PACE Institute of Technology and Sciences, Ongole, AP, India

Tanikonda Prasanth
UG Student, Department of Electrical and Electronics Engineering in Pace Institute of Technology and Sciences, Ongole, AP, India

Nakka Venkata Karthik
UG Student, Department of Electrical and Electronics Engineering in Pace Institute of Technology and Sciences, Ongole, AP, India

Puram Lohith Kumar
UG Student, Department of Electrical and Electronics Engineering in Pace Institute of Technology and Sciences, Ongole, AP, India

Yekollu Chakradhar
UG Student, Department of Electrical and Electronics Engineering in Pace Institute of Technology and Sciences, Ongole, AP, India

K. V. Narayana
Assistant Professor, Department of EEE, PACE Institute of Technology & Sciences, Ongole, AP, India

K Sowjan kumar
Assistant Professor, Department of EEE, PACE Institute of Technology & Sciences, Ongole, AP, India

Dr. Y.Prakash
Professor, Department of EEE, PACE Institute of Technology & Sciences, Ongole, AP, India

Dr. K. Venkateswarlu
Professor, Department of EEE, PACE Institute of Technology & Sciences, Ongole, AP, India

ABSTRACT
In this proposed paper, a novel nine-level inverter (NLI) topology is proposed, which uses fewer components to provide nine voltage levels in the output. Ten semiconductor switches, four capacitors, and one dc voltage source are included in this NLI. Through various logical arrangements of the dc source and capacitors and the use of power semiconductor switches, the nine voltage levels are generated. In this case, only two switches can conduct simultaneously in any mode. As a result, the system's efficiency is increased and conduction losses are decreased. The low total standing voltage (TSV) of the power semiconductor switches is another crucial aspect of this design. Gate signals are produced using a suggested modulation approach to lessen the power switches' switching loss. Several Simulink simulations are run in order to validate the NLI. The suggested inverter has a much lower requirement for components and dc sources as compared to conventional topologies. In order to increase the efficiency of the power generating process in renewable energy systems, the proposed NLI structure can be implemented.

1. INTRODUCTION
Over fossil fuels, renewable energy sources hold enormous promise. However, because of their poor power generation capacity, high cost, and space requirement, these sources are only used to a relatively limited extent. These restrictions depend heavily on the effectiveness and design of the inverter in a renewable energy system. As a result, numerous inverter designs are mentioned in the literature. Due to their low total harmonic distortion (THD) and low voltage stresses on switches, multilevel inverters (MLI) are attracting a lot of attention to operate in renewable energy systems [1].

Diode clamped MLI (DCMLI) [3], flying capacitors MLI (FCMLI) [4], and cascaded H-Bridge MLI (CHBMLI) [5] are the three MLI types that are typically reported. Due to its higher number of capacitors and unbalanced dc link voltages, the cascaded H-Bridge (CHBMLI) performs better than the FCMLI and DCMLI among these three MLIs [6]. However, the primary limitation of conventional CHBMLI is that as the number of levels in the output increases, the number of switches and dc sources used also exponentially increases [7].

To reduce the aforementioned shortcomings of the traditional CHBMLI, other topologies have been developed. A multilayer voltage source inverter (MLVSI), which can generate seven levels utilising a single dc voltage source and parallel capacitors, is suggested in [8] using a modulation-based technique. It is suggested in [9] to use a single DC voltage source and six power switches in a five-level packed U-cell (5-PUC) inverter.

In [10], a different cross switch based multilayer inverter (CSMLI) is suggested, where (n+1) dc sources and (n+1) switches are employed. [11] proposes an asymmetric nine level inverter design with two dc voltage sources that are different from one another. [12] proposes another asymmetric nine-level inverter scheme with a smaller device count that uses two separate dc sources. A switched-capacitor multilevel inverter (SCMLI), which creates nine voltage levels in the output from a single DC source, is presented in [13].

The number of voltage levels could still be increased, and the quantity of switches, capacitors, and dc voltage sources might be decreased. These will decrease the size of the filter, the need for transformers, and the price of production. This study introduces a novel nine-level inverter (NLI) that makes use of just one dc voltage source and fewer switches. The lower switching loss and total standing voltage (TSV) of this NLI are its key benefits.

2. MULTILEVEL INVERTER
In recent years, high power equipment has started to be used in a variety of industrial applications. Megawatt power levels are needed for several medium voltage utility applications and motor drives. It is difficult to connect just one power semiconductor switch directly to a medium voltage grid. This has led to the introduction of a multilevel inverter construction as a substitute

in medium and high power applications (Jose Rodriguez et al. 2007). The harmonic quality of the output voltage can be improved with this kind of inverter [11].

A multilevel inverter converts many levels of DC voltage into the desired AC voltage waveform. These DC voltages could possibly be equal or unequal. These DC voltages generate stepped waveform AC voltage. The inability to directly convert stepped waveforms to sinusoidal waveforms is a disadvantage of multilevel inverters. Sharp transitions can be seen in the multilayer inverter's staircase waveform. According to the Fourier series theory, this process produces harmonics in addition to the sinusoidal waveform's basic frequency (John Chiasson et al. 2003).

Compared to a traditional two-level inverter that makes use of high switching frequency PWM, a multilevel inverter has a number of advantages. A multilevel converter's appealing qualities can be summed up succinctly as follows:

Multilevel inverters can lower the dv/dt stresses in addition to producing output voltages with extremely little distortion. Consequently, issues with electromagnetic compatibility can be minimised.

Because multiple inverters generate less CM voltage, the stress on a motor linked to one of these drives can be minimised. Additionally, by utilising sophisticated modulation techniques, CM voltage can be removed.

Low distortion input current will be drawn by multilevel inverters.

High switching frequency PWM and fundamental switching frequency can both be used by multilevel inverters. It should be noted that reduced switching frequency typically translates into improved efficiency and lower switching loss.

The biggest problem with multilayer inverters is that there are more switches as there are more levels. The creation of control circuitry for numerous power switches was a critical issue in the early phases of multilayer inverters. Another flaw with this inverter is that it needs numerous DC voltage sources, most of which are provided by capacitors. A significant problem is balancing the voltage sources when they are operating under various load situations. Despite these negative aspects, the addition of multilevel inverters will reduce switching losses in the power device. A smaller size filter is needed to eliminate harmonics as compared to two level inverters. As a result, the inverter's weight, size, and price are decreased. Over the past 20 years, numerous multilevel inverter topologies have been proposed. Modern research has led to the development of novel inverter topologies and distinctive modulation strategies. Furthermore, the literature has reported on three different significant multilevel inverter structures. It's them, flying capacitors/capacitor clamped multilevel inverters, cascaded H-bridge multilevel inverters, and diode clamped/neutral clamped multilevel inverters are a few examples.

Table 1: Traditional two-level and multilayer inverters are compared

S.NO	Conventional Inverter	Multilevel Inverter
1	THD in output voltage is higher	Low THD in output voltage
2	More switching stresses on Devices	Reduced switching stresses on devices
3	Not applicable for high voltage Applications	Applicable for high voltage applications
4	Higher voltage levels are not Produced	Higher voltage levels are produced
5	Since dv/dt is high, the EMI from system is high	Since dv/dt is low, the EMI from system is low Lower
6	Higher switching frequency is used hence switching losses is high	Lower switching frequency can be used and hence reduction in switching losses
7	Power bus structure, control schemes are simple	control scheme becomes complex as number of levels improved
8	Reliability is high	Reliability can be improved, rack swapping of levels is possible

3. PROPOSED INVERTER AND MODULATION TECHNIQUE

Proposed NLI structure shown in Fig. 1 can generate nine level in the output voltage across load by dint of a dc voltage source (Vdc), ten power semiconductor switches (S1- S10) and four capacitors (C1-C4)

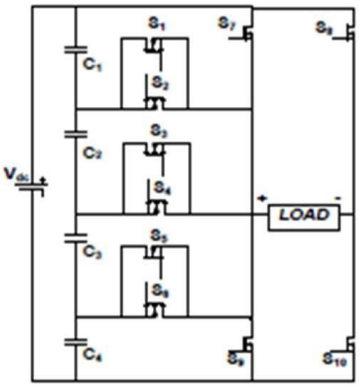
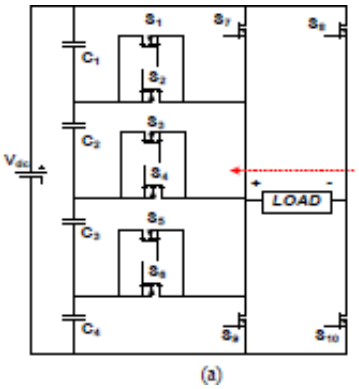


Figure 1: Proposed topology for nine level inverter (NLI)

Here, 10 switches are utilised to create various combinations between the four capacitors that are connected in series to divide the dc voltage source into four equal parts (Vdc/4) to provide various output voltage levels. In order to examine the voltage levels across the linked resistive load of the proposed NLI, various current routes for various switching configurations are shown in Fig. 2. Here, the dashed red line indicates the load current. All the switches are initially off to provide a zero voltage level. As seen in Fig. 2(a), all four capacitors are then charged to a voltage equal to one-fourth of the dc voltage source (Vdc/4).

The current path at that point is shown in Fig. 2(b) as switch numbers S5 and S10 are turned ON to provide the first positive voltage level in the output. The second positive voltage level (Vdc/2) is created by keeping switches S3 and S10 on. The current path for this is indicated in Fig. 2(c), and during this period, two capacitors, C3 and C4, are discharged simultaneously. By turning on switches S1 and S10 where C2, C3, and C4 will be discharging, the third positive voltage level (3Vdc/4) shown in Fig. 2(d) is created.



(a)

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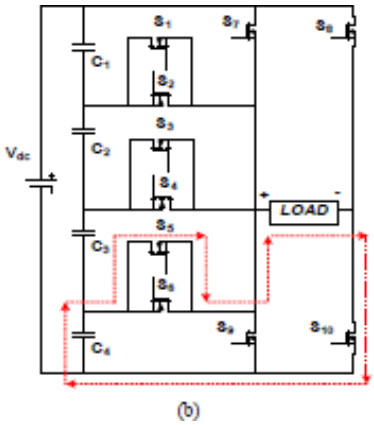

(b)

Figure 2: The projected NLI topology's various voltage levels

(a) Vout = 0 (b) Vout = Vdc/4,

Table 2: Generated output voltages of the suggested nine-level inverter under various switching situations

Ser		ON Switches	V_o
Switching States	1.	S_7, S_{10}	V_{dc}
	2.	S_1, S_{10}	$3V_{dc}/4$
	3.	S_3, S_{10}	$V_{dc}/2$
	4.	S_5, S_{10}	$V_{dc}/4$
	5.	All switches OFF	0
	6.	S_2, S_8	$-V_{dc}/4$
	7.	S_4, S_8	$-V_{dc}/2$
	8.	S_6, S_8	$-3V_{dc}/4$
	9.	S_8, S_9	$-V_{dc}$

As indicated in Fig. 2(e), the fourth positive voltage level (Vdc) is produced by turning on switches S7 and S10. Then, by turning on switch number S2, the first negative voltage level (Vdc/4) is produced, and capacitors C2, C3, and C4 are now discharged, as shown in Fig. 2(f). To create the second negative voltage level (Vdc/2), when capacitors C3 and C4 are discharged, switches S4 and S8 are turned ON. This state is seen in Fig. 2(g). Turning on switches S6 and S8 causes the capacitor C4 to discharge, creating the third negative voltage level (3Vdc/4) and the current flow depicted in Fig. 2(g). By turning ON switches S8 and S9, where no capacitors are present in the current flowing channel as illustrated in Fig. 2 (i), the fourth negative voltage level (Vdc) is finally achieved. In this manner, ten switches, one dc voltage source, and a total of nine voltages levels—four positive, four negative, and one zero level—are produced. In order to achieve the requisite nine output voltage levels, the ON states of 10 switches are summarised in Table I.

4. PLANNED MODULATION TECHNIQUE

A modulation Nine levels will be created in the output of the suggested NLI using a modulation technique. Fig. 3 and Fig. 4 demonstrate, respectively, the modulation method and the turning ON pulses for the ten switches. The turning ON pulses for S1 to S8 switches are produced by matching an eight-level dc voltage range with a modulating (reference) wave |VmSint|.

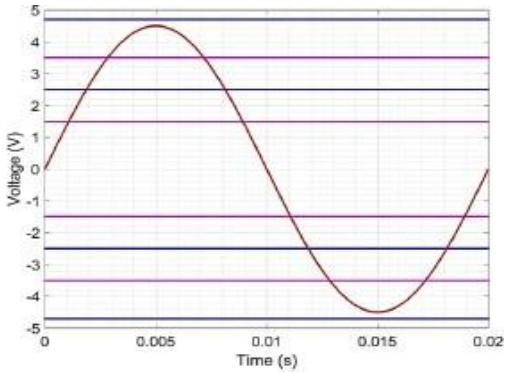

Figure 3: Modulation strategy of the proposed NLI topology

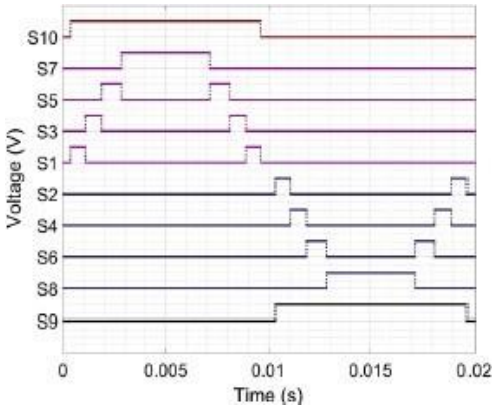

Figure 4: Pulses that turn on the 10 switches

The modulating wave is compared to the level of zero dc voltage to provide gate pulses for S10 and S9. It should be noted that switch S10 controls the upper half of the modulating wave while switch S9 controls the lower half. The low switching frequency of the pulses, which is the same as the frequency of the modulating wave, is the primary characteristic of this modulation method.

5. SIMULATION RESULTS

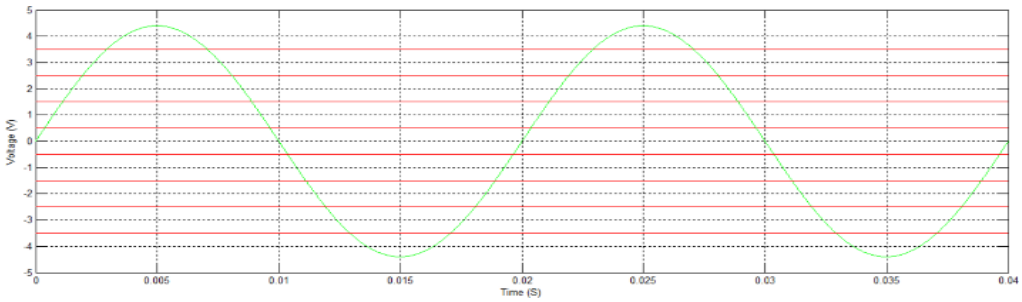

Figure 5: Method for modulating the proposed NLI topology

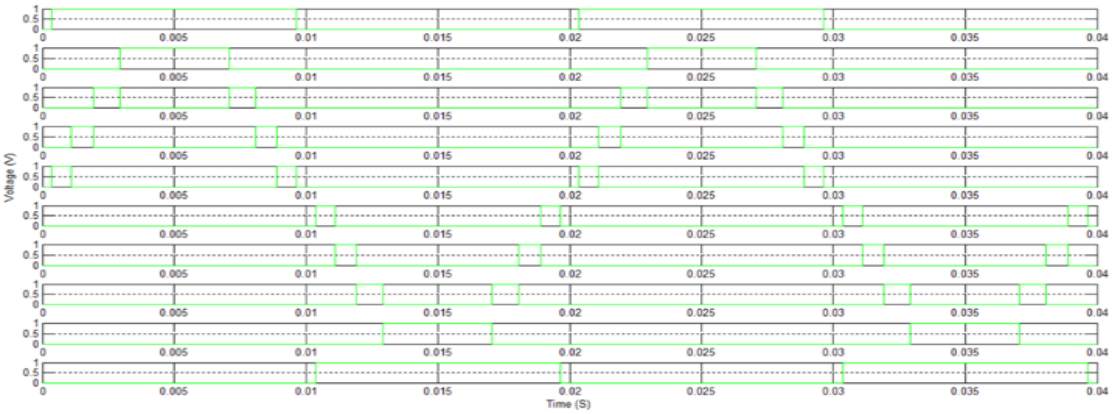

Figure 6: Turning ON pulses for the ten switches

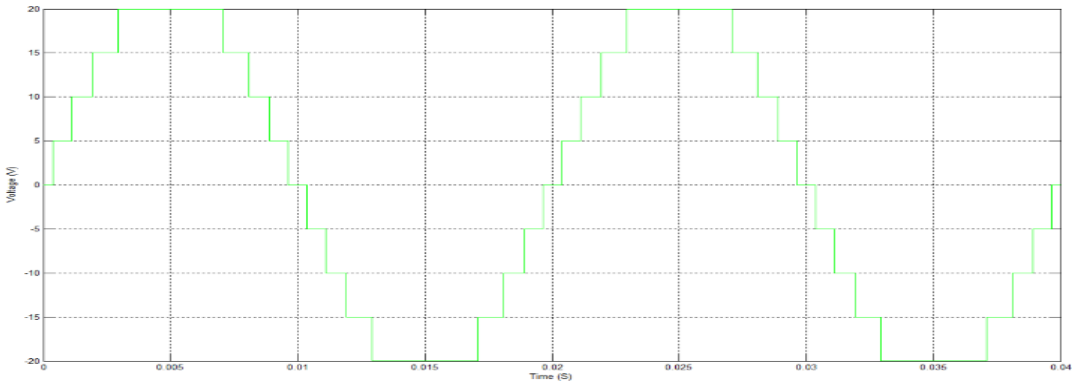

Figure 7: Nine voltage levels in the output waveform of the simulated NLI in 50Hz frequency with R-load

6. CONCLUSION

A This project introduces a multi-level inverter (MLI) that can produce nine voltage levels in the output. The need to create an effective inverter for renewable energy systems is established at the outset of the project. Literature on various inverter types is researched to determine the best design strategy. Then, an entirely new nine-level inverter (NLI) topology is presented, complete with a switching table and all nine steps. The process for modulating the gate pulses is then explained. Finally, the output waveform's nine levels are detailed together with its FFT, confirming the viability of the suggested NLI structure. Without any filtering, the output's THD was 9.38%. The key benefits of this topology are the power semiconductor devices' lower switching loss and lower overall standing voltage. Due to the fact that only two switches are switched ON at once to produce various voltage levels, this NLI has fewer conduction losses. The process of producing renewable energy will therefore be more effective thanks to this NLI framework. The implementation of an experimental design is currently underway, and future communications will give more analysis of the design's execution and experimental findings.

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