International Journal of Innovative Research in Computer Science & Technology (IJIRCST)
ISSN: 2347-5552, Volume-9, Issue-6, November 2021
https://doi.org/10.55524/ijircst.2021.9.6.20
Article ID IRPS12030, Pages 86-90
www.ijircst.org

A Review Paper on the Difference between Single-Cycle and Multi Cycle Processor

Madhav Singh Solanki[1], and Ms Anuska Sharma[2]

[1 ,2] SOEIT, Sanskriti University, Mathura, Uttar Pradesh, India

Correspondence should be addressed to Madhav Singh Solanki; madhavsolanki.cse@sanskriti.edu.in

ABSTRACT- The processors are all important components of computer architecture. Computer architecture is a specification that describes how hardware and software technologies are connected to create a computer platform. It refers to a system that processes any fetched instruction. There are many different types of processors, and we shall examine the distinctions between single cycle and multi-cycle processors in this article. Former processors only executed an instruction in a single clock cycle, while multi-cycle processors disassembled the instructions into multiple functional pieces and then executed each portion in a separate clock cycle. Because the multicycle processor breaks down each instruction into smaller pieces, the amount of hardware required is decreased, and several registers are added to store data that may be utilized in the execution of subsequent instructions. A multicycle processor executes instructions in smaller clock cycles than a single cycle processor, according to the proposed study.

KEYWORDS- Arithmetic Logical Unit, Computer Architecture, Microprocessor, Multi-Cycle Processor.

I. INTRODUCTION

A. Computer Architecture

Computer architecture and design are one of the prominent advancing fields of technology, and within the increasing use of processing devices on daily basis; the goal is to establish a balance between performance and power consumption. Computer architecture is a specification that describes how software and hardware interconnect with each other to construct a computer platform. When the word architecture is thought of, all the buildings, houses, monuments, etc. strike into our minds. Keeping all the above things in mind, we can state that computer architecture includes building of computers and all other parts that go into a system. Computer architecture has three main categories [1].

B. System Design

The process of defining elements of a system and their interface is called system design. This design includes all the hardware parts i.e. central processing unit (CPU), memory, data processors, multiprocessors, controllers, and direct memory access. All this comes under actual Computer system. System design uses top to bottom or bottom-to-top approach to take all the records of related variables of the system. It satisfies all the specific needs and requirement of a business or organization via engineering of logical and well off running system. Similarly, Circuit Design, scrutinize in
detail the background and coding techniques of VHDL, including its code structure, concurrent , operators, attributes, concurrent and sequential statements and code, objects (signals, variables, and constants), design of finite state machines, and examples of additional circuit designs [2].

C. Instruction Set Architecture

Instruction set architecture (ISA) defines program visible components and specifications it includes all the functions, capabilities, data formats, processor register etc. that are used by a computer system. ISA provides command to the processors, to tell what it needs to do. All processors can have same instruction set but still can have different internal design. Examples of ISA are:

- ADD – add two numbers together
- JUMP – jump to desired RAM address
- LOAD – load information to CPU
- STORE – store information to RAM
- BRANCH - offset the address in program counter

D. Micro Architecture

The implementation of all the data processing and storage elements or data paths into instruction sets are defined by micro architecture for example all the DVD devices and similar ones. It includes the design of the instruction pipeline its execution technique, caches. It also defines the technology and base materials used for the building up of transistors, electronic components and interconnect[3].

E. Processor

Complete design of 32-bit, single cycle (MIPS) consists of two interacting parts:

- 32-bit data path
- Control unit.[4].

The program counter is used to jump onto the next instruction to be executed [5]. The hardware executes the instructions or computer programs stored in the memory. The central processing unit of a computer handles all basic system instructions such as mouse processing, inputs of the keyboard, running applications etc. Most central processing unit (CPUs) that receives instruction from both hardware and active software and produces output accordingly are developed by either Intel and uses the x86-processor architecture. Mobile devices for example cellular phones, laptops, iPad, tablets can use Intel or AMD as processors but they specifically include the usage of processors developed by ARM and Apple. Besides the main processing unit, mobile devices include Graphical processing unit (GPU). GPU is an electronic circuit, which renders graphics that are output on a monitor screen. GPUs are usually present on the video cards in desktops, whereas graphics cards are integrated into the motherhood in mobile devices. There are separate processors for graphics and other running apps hence the processing quality of different applications are not deteriorated [6].

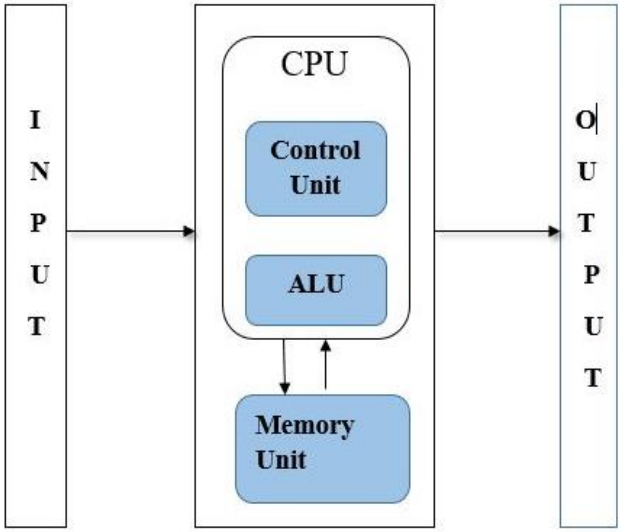

Figure 1: Processing unit showing how the request or data is processed using different components of central processing unit.

There are two types of processors, which will be discussed in this proposed work i.e. single cycle, and multicycle processor. A "Datapath" shows the complete execution of processors. Single cycle processor is a processor in which the instructions are fetched from the memory, and then executed, and the results are further stored in a single cycle, whereas in multicycle implementation, each step in execution takes one clock cycle. As long as it is used on different clock cycles, it allows the functional unit to be used more than once per instruction. Execution of both the processes can be implemented using high-speed integrated circuit hardware description language (VHDL). Presence of synthesis tools that helps to convert HDL logic to FPGA primitives has formed HDL the digital design entry method of choice [7]. Figure 1 shows the Processing unit showing how the request or data is processed using different components of central processing unit.

Single cycle MIPS Computing RISC processor that can executes an complete instruction in single cycle [8]. Single cycle implementation executes in a single clock cycle. The RISC processor has fixed-length of 32-bit instructions based on three different format J-format, R-format and I-format, and 32-bit general-purpose registers with memory word of 32-bit [9].

F. Multi Cycle Processor

The multi-cycle MIPS data path is very similar to the single-cycle MIPS data path with a few additions[10]. The Multi cycle processors contain various registers to hold data temporarily from the previous clock cycle. These include an Instruction register, ALU out, Memory data register, etc. In the implementation each instruction is broken into shorter parts, these smaller instructions are stored in registers especially induced for this work. This implementation executes the simpler instructions faster and the expensive hardware can be used repeatedly. This makes the system more efficient and economical. There are five extra registers, which are especially introduced to store the functional broken parts of each instruction in multicycle data path.

G. Data Path

A data path is an assembly of all the functional units, such as ALU, decoders and multiplexers that are used to perform all data processing or calculating operations. Data path is the framework of how an instruction flow takes place. Along with data path, control signals are attached. These control signals determine the command that has to be fetched in the next components. The methodology, which will be used for constructing the data path, is as follows:

- Read instructions from memory
- Decode the instruction and read two registers that the instruction might use
- Perform the arithmetic and logical calculations or access memory
- Write back the result to the register file using write port
- Determine the next value of PC (Program counter) and update PC for next instruction

Single cycle and multicycle processors have different data path depending upon the components. Components of data path are as follows -

- Memory
- Program counter
- Instruction Register
- Memory data register
- Register File
- Arithmetic and logic unit (ALU): ALU comprises of two function units and performs all the logic operations such as AND, NAND, OR, NOR, XOR, XNOR and ADD OR SUB.

These components are implemented using VHDL language on XILINX software. VHDL is used in electronic automation systems to describe digital and

mixed signal such field programmable gate arrays (FPGA) and integrated circuits.
Refereeing to Figure 2 MIPS instructions are executed in three to five steps as follows:

- **IF**
  Fetch the instruction from memory
- **ID**
  Decode every instruction and generate control signals
- **EX**
  Control signals are fed into ALU to get results
- **REM**
  Read from memory
- **WB**
  Write back the result into register file

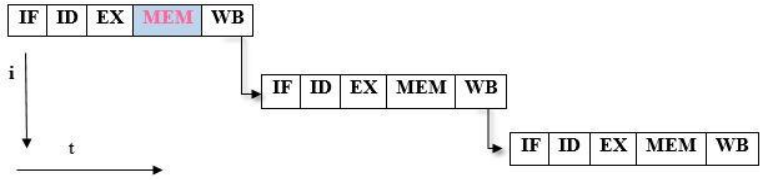

Figure 2: Execution flow of Microprocessor without Interlocked Pipelined Stage instructions by dividing each cycle into smaller parts and following the pipeline method

The author has used VHDL language for implementation using the XILINX platform. Xilinx software is a package of software tools, which are used to design a digital circuit and implemented the digital circuits using Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD). VHDL stands for VHSIC (very high-speed integrated circuit) hardware descriptive language. VHDL includes library and syntax same as C and C ++ language. VHDL is a multi-purpose language that is used for documentation, verification and synthesis of large digital design. VHDL has three different approaches to define hardware i.e. structural, dataflow and behavioural methods of hardware description. In general all three approaches are mixed and then a final code is designed .This language can be implemented on various software such as MULTISIM, XILINX etc. In this paper, the author has used XILINX software as shown in Table 1.

Table 1: shows the comparison between CPI, Speed up, Clock Period, Program Execution Time and Clock Cycle Number

PROCESSOR	CPI	SPEED UP	CLOCK PERIOD	PROGRAM EXECUTION TIME	CLOCK CYCLE NUMBER
MULTICYCLE MIPS	4	1.25	2,398 ns	4	1.25 599.5

II. DISCUSSION

A pattern of waveforms is generated which shows how much time each instruction takes to complete its execution time The snapshot from figure 3 is the result of code executed of each instruction and also analysing the clock cycle time of each instruction. The above image shows the execution time of LW, SW. Load, Store, and branch instructions that show less execution time and decreased clock cycles. Above table 2 compares the show that a multicycle processor takes a lesser amount of time than single-cycle processor which in turn results to be an efficient processor. Multicycle processor enhances the use of hardware as one register can be used to store data that can further uses in another instruction execution. It is a parallel execution process and we do not need to store the values, the moment it is available these values are consumed and the instruction is executed thereafter. Cycle time of a single cycle processor is eight ns.
Propagation delay must be lengthy enough to accommodate instruction in a single cycle. Arithmetic instructions such as addition and subtraction of operators i.e. ADD, SUB executes quickly and time is wasted in each cycle, whereas jump instructions, which store and write back the information into register file LW, SW, Load have much longer propagation delay.

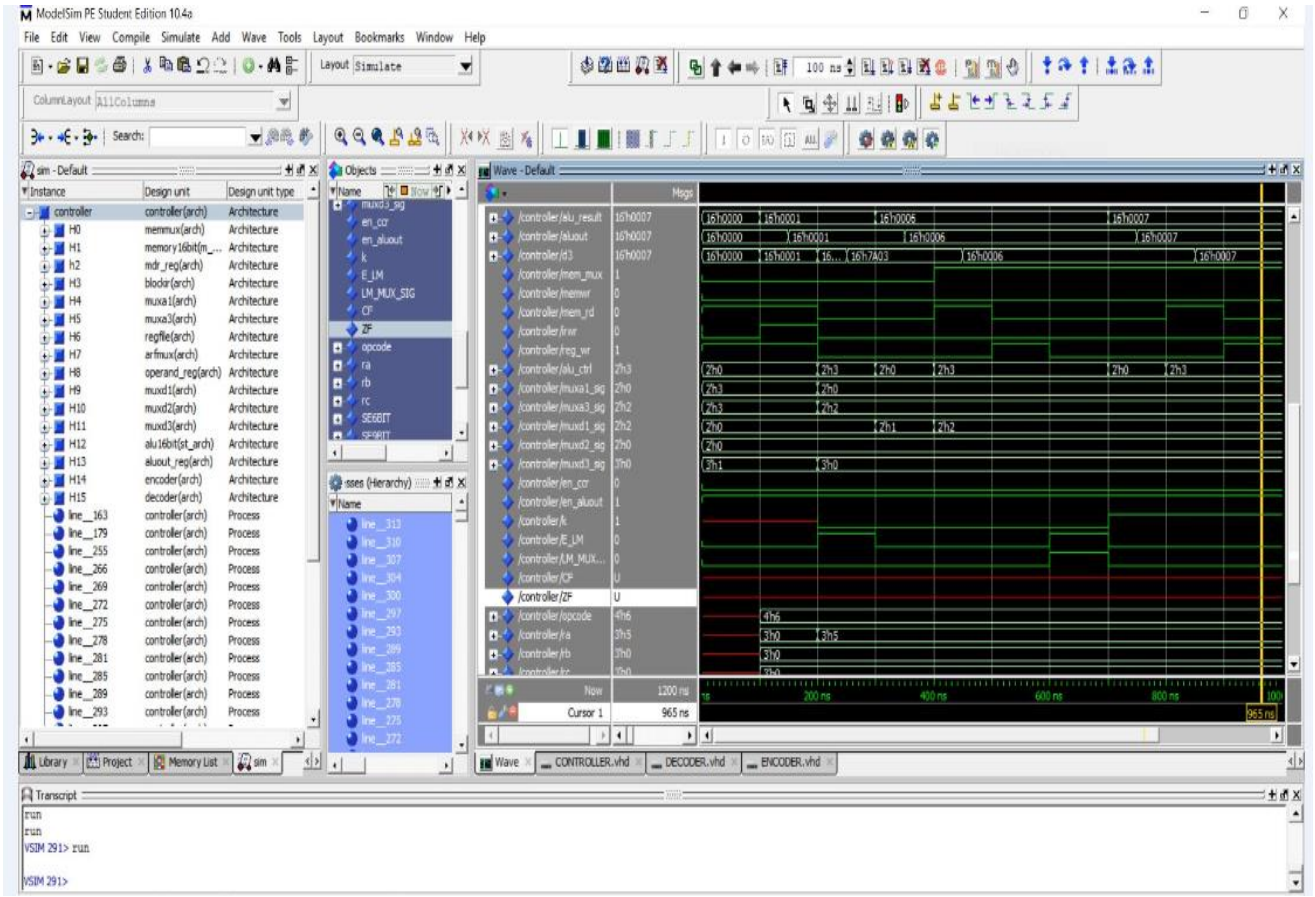

Figure 3: Waveform snapshot explaining the execution of ADD, SUB, LW, SW, Branch instruction and also representing the time taken and clock cycle taken

Table 2: Shows the Comparison between execution times, Clock cycle, Speed up of both single and multicycle processor.

PROCESSOR	CPI	SPEED UP	CLOCK PERIOD	PROGRAM EXECUTION TIME	CLOCK CYCLE NUMBER
SINGLE CYCLE MIPS	1	1	20	3,000 ns	150
MULTICYCLE MIPS	4	1.25	4	2,398 ns	599.5

III. CONCLUSION

The single-cycle MIPS processor contains two prominent drawbacks. Firstly, the clock cycle must be lengthy enough to provide support to the slowest instruction i.e. (LW). Second, functional units cannot be used more than once per instruction. Therefore, the single-cycle MIPS processor requires two adders in addition two ALU and separate instruction and data memories, which in turn raise the implementation cost. The multicycle processor in scripts the disadvantages by fragmenting each instruction into small or shorter steps of each clock cycle corresponding to the functional unit operations that are needed. This permits instructions to take various other numbers of clock cycles and functional units can be shared within the execution of a single instruction. Therefore, compared to the single-cycle implementation the multicycle implementation of a processor uses smaller design modules and some faster or higher speed clocks.

REFERENCES

[1] Shi J, Gao F, Wu TJ. Single-cycle and multi-cycle generalized 2D model predictive iterative learning control (2D-GPILC) schemes for batch processes. J Process Control. 2007;

[2] Pedroni V. Circuit Design with VHDL. MIT Press. 2004.

[3] Koledina KF, Koledin SN, Gubaydullin IM. Optimal conditions for single-cycle and multi-cycle reactions

based on a kinetic model. In: Journal of Physics: Conference Series. 2018.
[4] Safaa S. Omran Hadeel S. Mahmood. No Title. ICIT 2013 6th Int Conf Inf Technol. 2013;
[5] Dennis DK, Priyam A, Virk SS, Agrawal S, Sharma T, Mondal A, et al. Single cycle RISC-V micro architecture processor and its FPGA prototype. In: 2017 7th International Symposium on Embedded Computing and System Design, ISED 2017. 2018.
[6] Xu SZ, Wang LW, Wang RZ. Thermodynamic analysis of single-stage and multi-stage adsorption refrigeration cycles with activated carbon-ammonia working pair. Energy Convers Manag. 2016;
[7]. Hardware Description Language: Verilog. In: Introduction to Embedded System Design Using Field Programmable Gate Arrays. 2008.
[8] Safaa S. Omran HSM. HARDWARE MODELLING OF A 32-BIT, SINGLE CYCLE RISC PROCESSOR USING VHDL. ICIT 2013 6th Int Conf Inf Technol. 2013;
[9] Reaz MBI, Jalil J, Rahman LF. Single core hardware modeling of 32-bit MIPS RISC processor with a single clock. Res J Appl Sci Eng Technol. 2012;
[10] Mohammad Zaid PPM. DESIGN AND APPLICATION OF RISC PROCESSOR. Impact. 2017;