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2:1 Multiplexer Design Using Lector, LCnmos, LCpmos Power Reduction Techniques with 45nm, 90nm, 180nm CMOS Technology

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ABSTRACT- Today's modern communication requires high data transmission rate and low power consumption. One of the most common concept of data transmission can be achieved by Multiplexers. The Multiplexers are the logic designs where data can be transmitted by n number of inputs over transmission path based on the selection line producing the single input. The application of Multiplexers is more active in communications system. AlsoLow power consumption and high-speed result is the major concern for choosing the digital circuits [1,2].
Here we designed 2:1 Multiplexer using CMOS technology with 45nm, 90nm, 180nm. Since CMOS offers less power consumption, we can till reduce the power consumed by using power reduction techniques. In this paper we designed and compared the 2:1 Multiplexer using Lector, LCnmos and LCpmos power reduction techniques.

KEYWORDS- Multiplexer, CMOS technology, Lector technique, LCnmos technique and LCpmos technique.

I. INTRODUCTION

A combinational circuit in digital electronics defines as the circuits whose output depends upon on the combinational input variables.
The combinational circuits have some of the special characteristics such as:

- no memory required
- no feedback
- 'm' number of outputs are obtained by 'n' number of combinational inputs.

Examples of common combinational logic circuits include: half adders, full adders, multiplexers, de-multiplexers, encoders and decoders [3,4].
The below figure 2, represents the general block diagram representation of Combinational circuit for 'm' number of outputs for 'n' combinational inputs

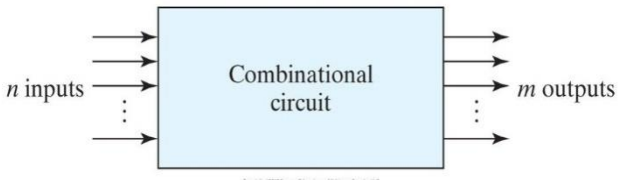

Figure 1: Block diagram of combinational circuit

II. MULTIPLEXER

One of the most used combination circuits is the MULTIPLEXER, also known as MUX.A Multiplexer is a combinational circuit, which has 2^n inputs, a single line output and n number of selection lines. The output of the multiplexer depends upon the selection lines Multiplexers are of many types i.e 2:1 mux, 4:1 mux, 8:1 mux, 16:1 mux and many more[5,6,7].
The Boolean expression for 2:1 multiplexer is given as:
$Z = A.(\text{not})S_0 + B.S_0$

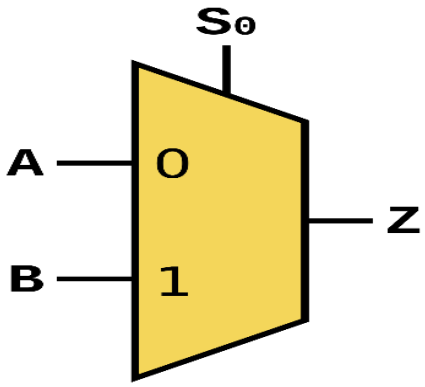

Figure 2: Block diagram of 2:1 multiplexer

Multiplexer is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.
A 2-to-1 multiplexer consists of two inputs A and B, one select input S_0 and one output Z. Depending on the select

signal, the output is connected to either of the inputs. Since there are two input signals, only two ways are possible to connect the inputs to the outputs, so one selects needed to do these operations. If the select line is low, then the output will be switched to Ainput, whereas if select line is high, then the output will be switched to B input. The below figure shows the block diagram of a 2-to-1 multiplexer which connects two 1-bit inputs to a common destination.

Table 1: 2:1 Multiplexer truth table

S	Z
0	B
1	A

The applications of Multiplexer can be seen in Communication Systems, Computer Memory, Telephone Network, Arithmetic logic unit, Serial to parallel converter.

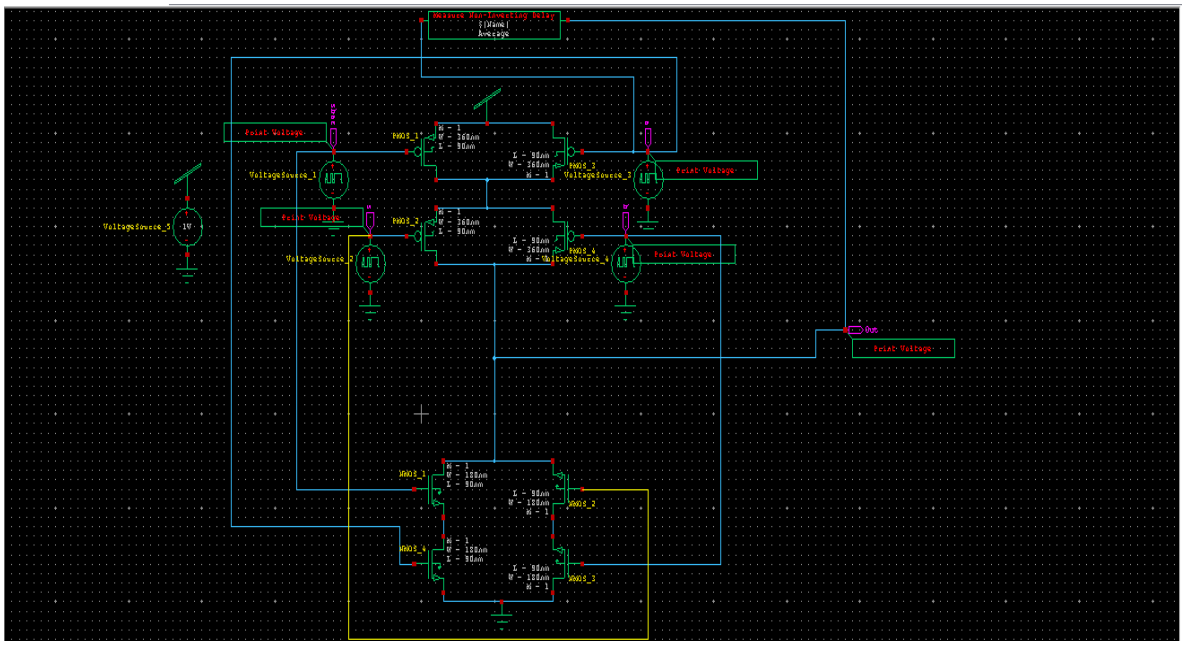

Figure 3: 2:1 Multiplexer using CMOS

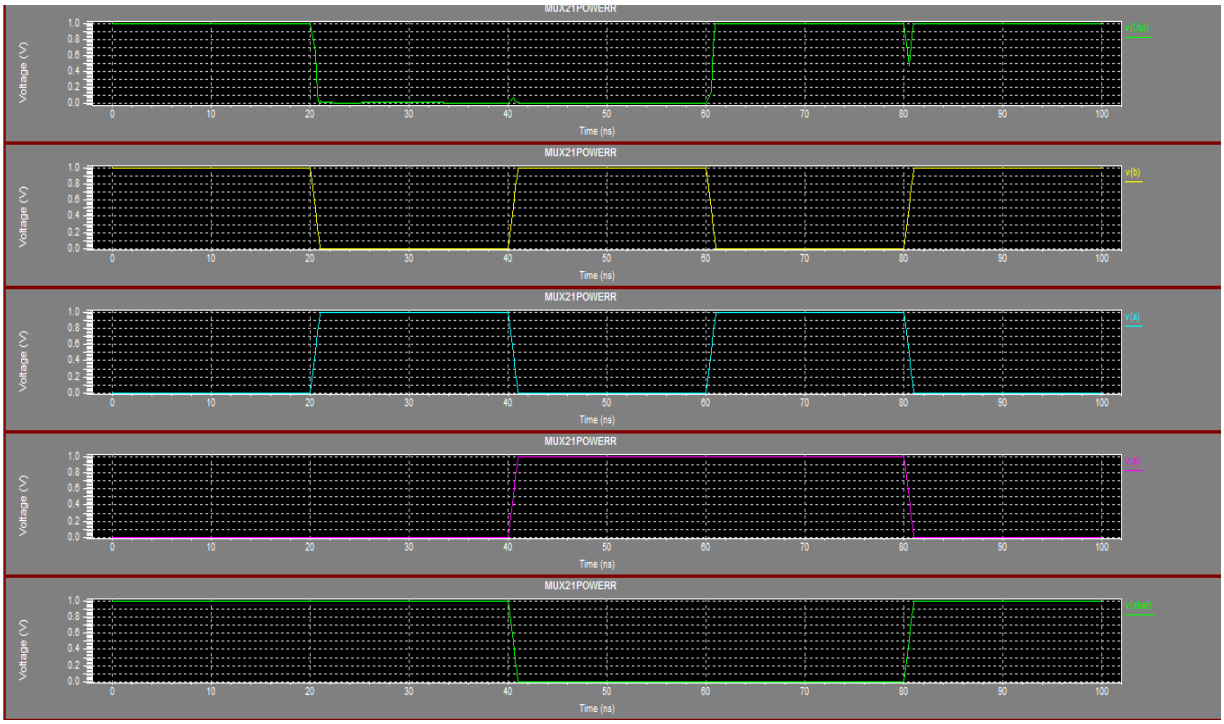

Figure 4: 2:1 Multiplexer output waveform for 180nm

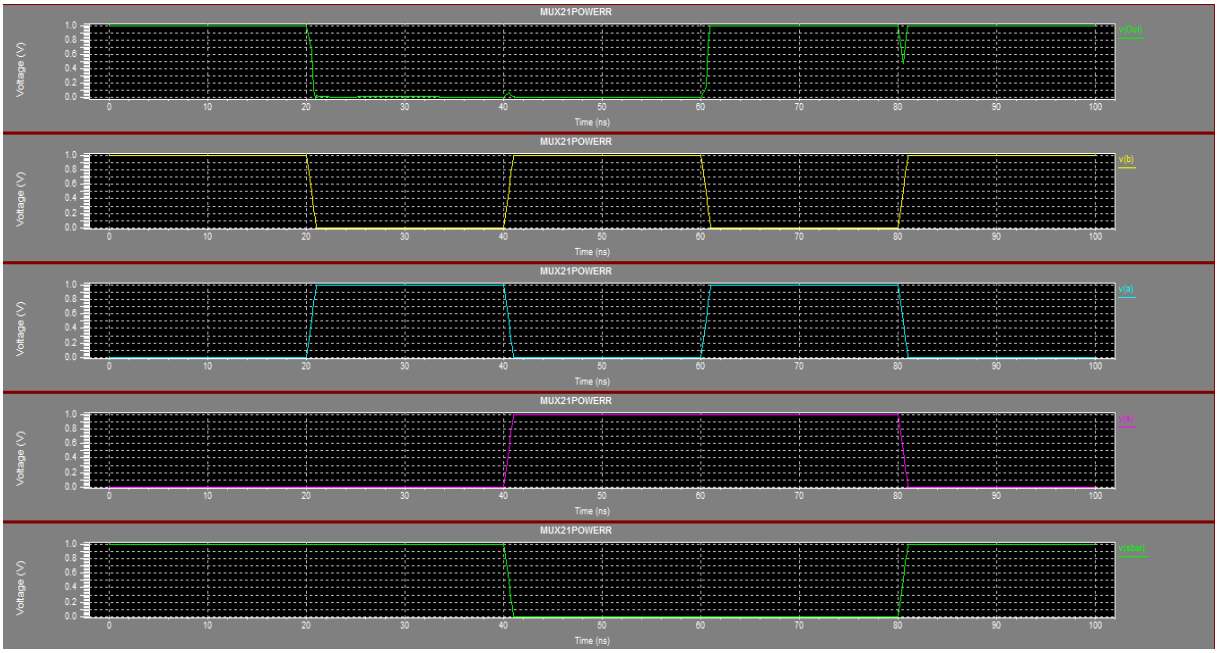

Figure 5: 2:1 Multiplexer output waveform for 90nm

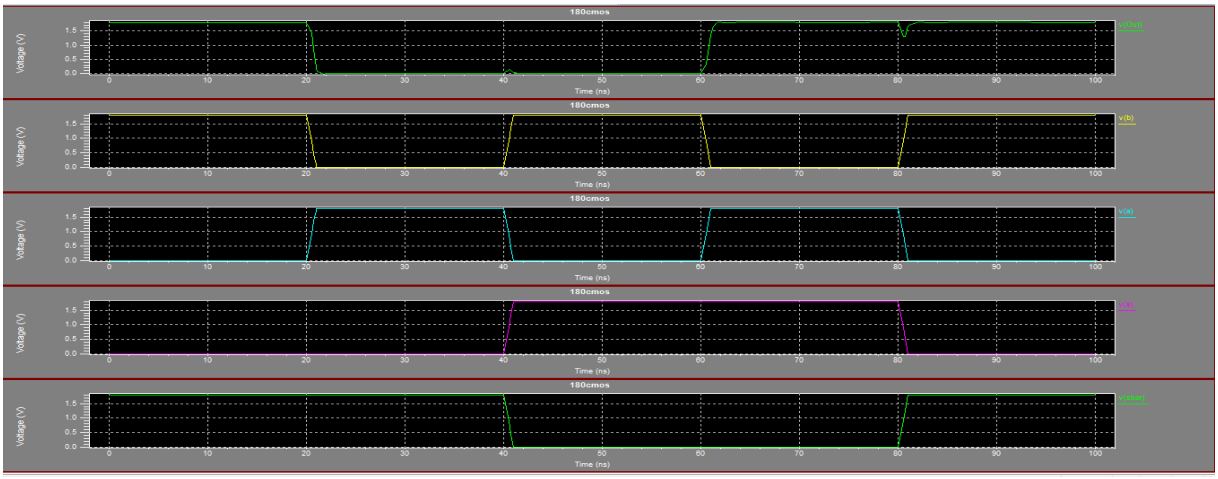

Figure 6: 2:1 Multiplexer output waveform for 45 nm

III. POWER REDUCTION TECHNIQUES

Low power design is a necessity today in all integrated circuits. As companies, started packing more and more features and applications on the battery-operated devices, battery backup time became very important. Power consumption slowly became an increasingly important criterion from the customers. Due to this, all chip companies are focusing on lower power consumption. There are efforts to reduce dynamic as well as static power consumption. Companies started to reduce the nominal voltages inside the chip, however, this was also limited along with the technology. So a lot of low power design techniques started to get employed during the Chip Design process to reduce both static and dynamic power consumption. Here in this paper we are going to discuss the three major power reduction techniques such as Lector, LCnmos, LCpmos.

A. L Cnmos Technique

The LCnmos is a leakage current power reduction technique in which an additional nmos is placed after the pull-down section, therefore, reducing the leakage power. It is a self-controlled nmos transistor, which does not require any other additional input. Only the output is feedback to the nmos[8,9].

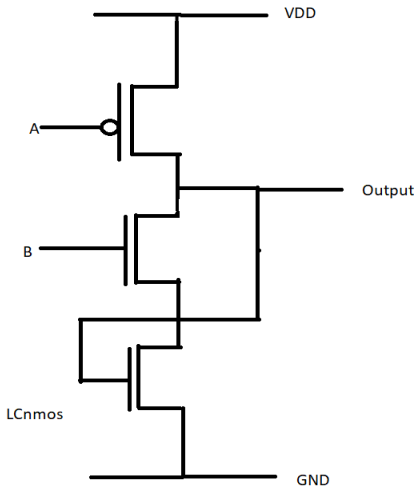

Figure 7: CMOS inverter using L Cnmos

The above figure 7, represents the L Cnmos of the CMOS inverter. Here the inputs are A and B. The output of the CMOS inverter is feedback to the additionally placed nmos below the pull-down.

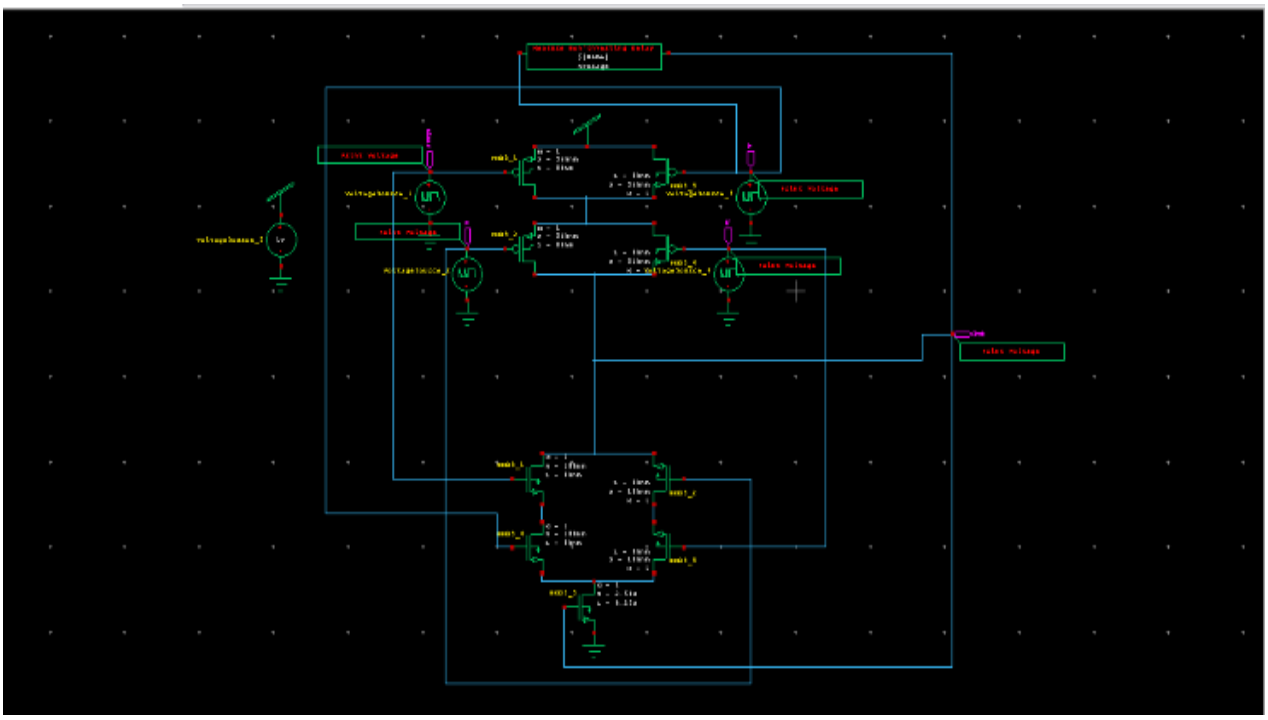

Figure 8: 2:1 Multiplexer using L Cnmos technique

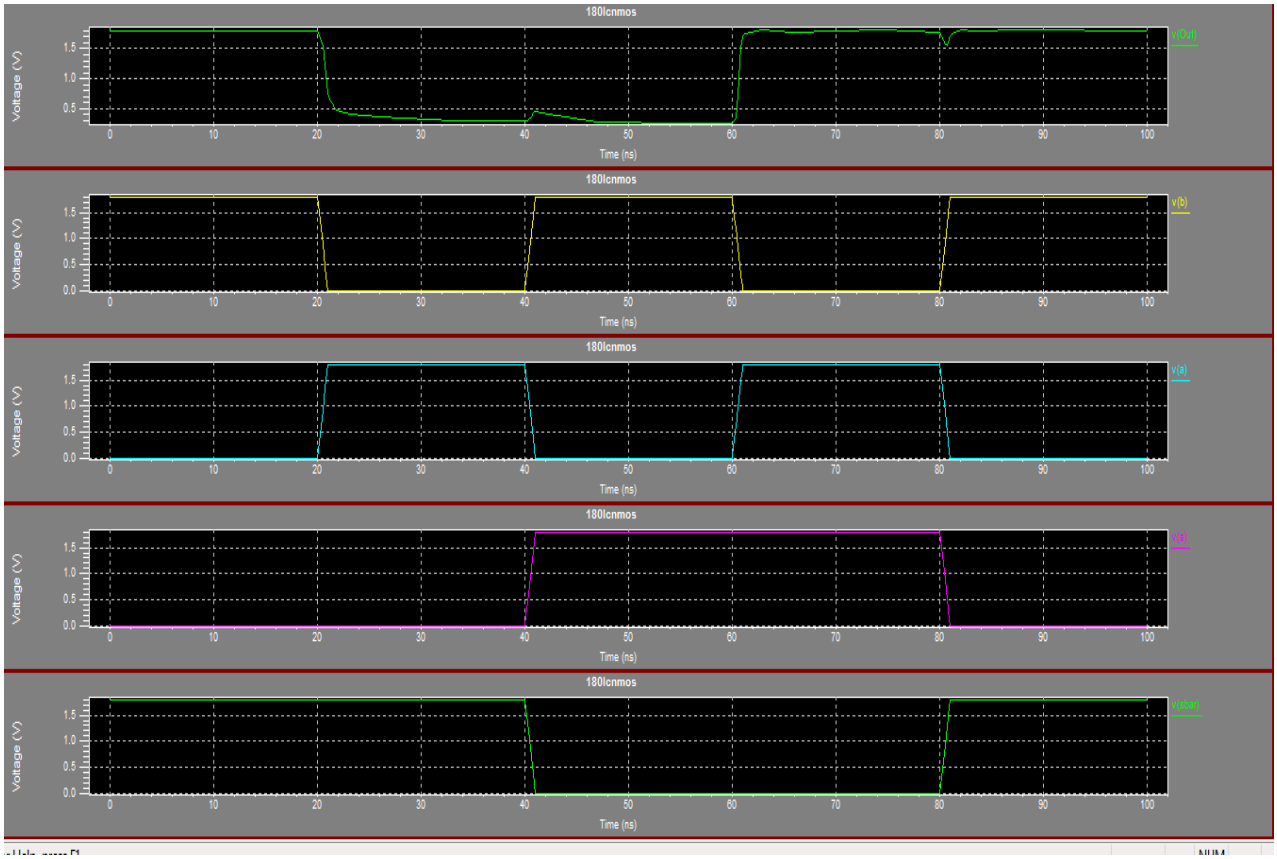

Figure 9: 2:1 Multiplexer output waveform for 180nm

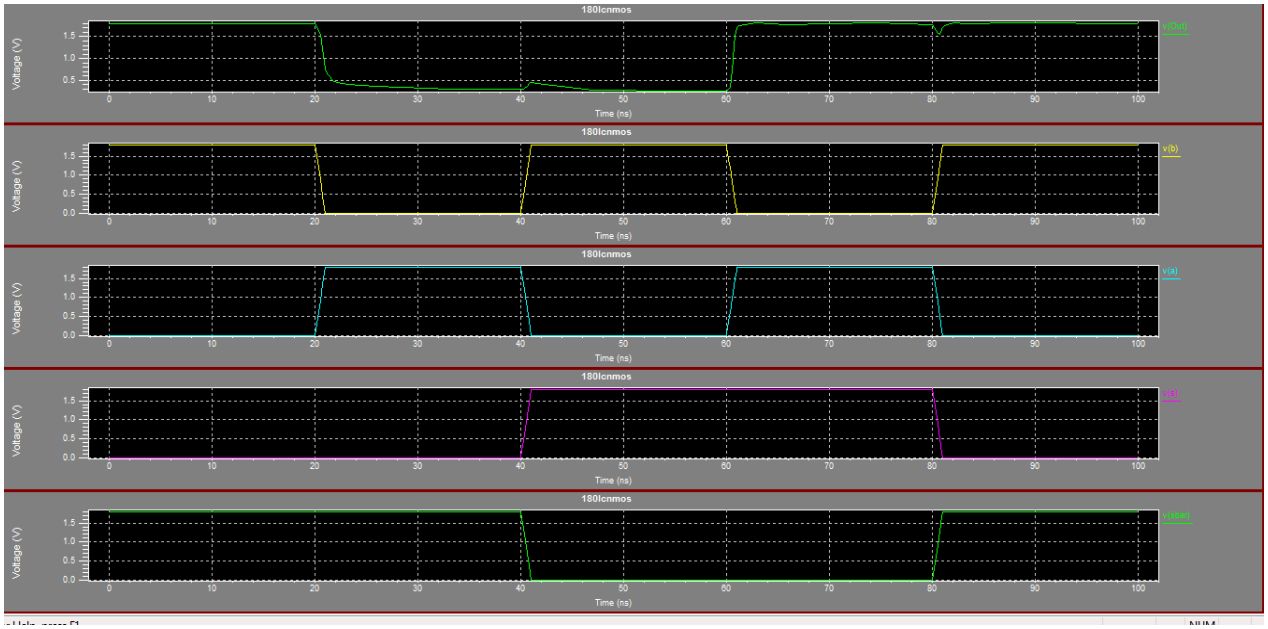

Figure 10: 2:1 Multiplexer using LCnmos with 90nm

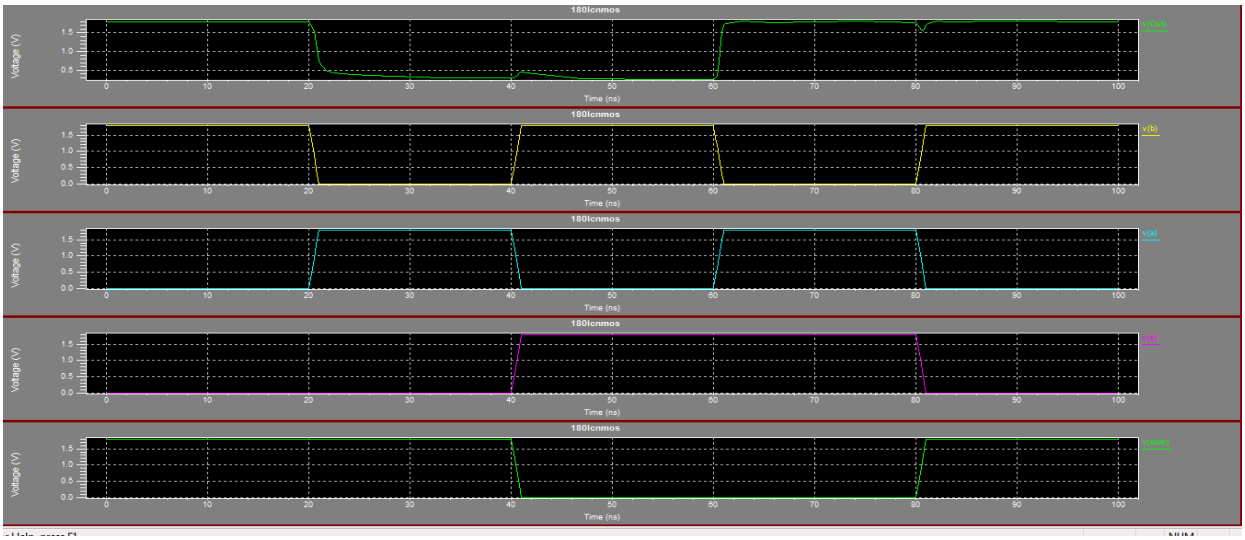

Fig.11: 2:1 Multiplexer using LCnmos with 90nm output

B. L Cpmos Technique

The LCpmos is a leakage current power reduction technique in which an additional pmos is placed after the pull-down section therefore reducing the leakage power. It is a self-controlled pmos transistor which does not require any other additional input. Only the output is feedback to the pmos[10,11].

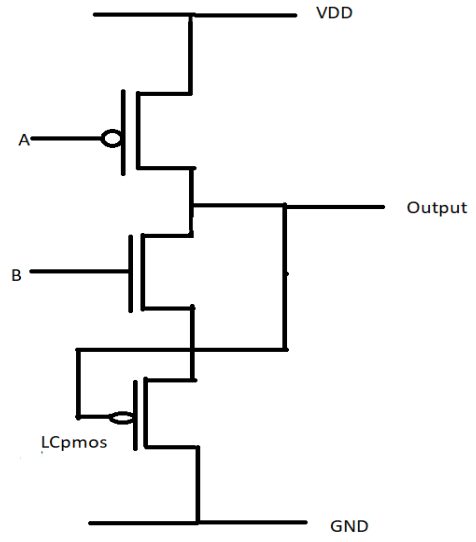

Figure 10: CMOS inverter using L Cpmos

The above figure 10, represents the LCpmos of the CMOS inverter. Here the inputs are A and B. The output of the CMOS inverter is feedback to the additionally placed pmos below the pull-down.

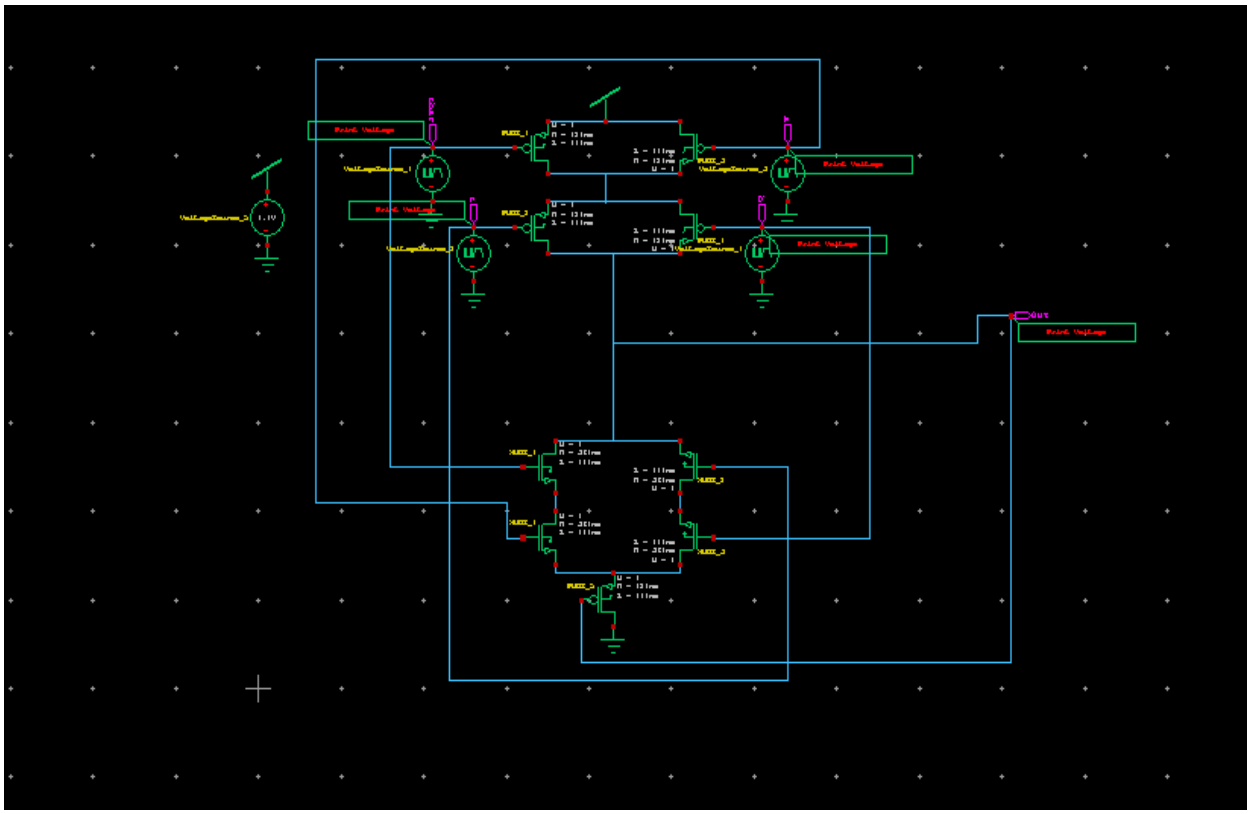

Fig.12: 2:1 Multiplexer using LCpmos technique

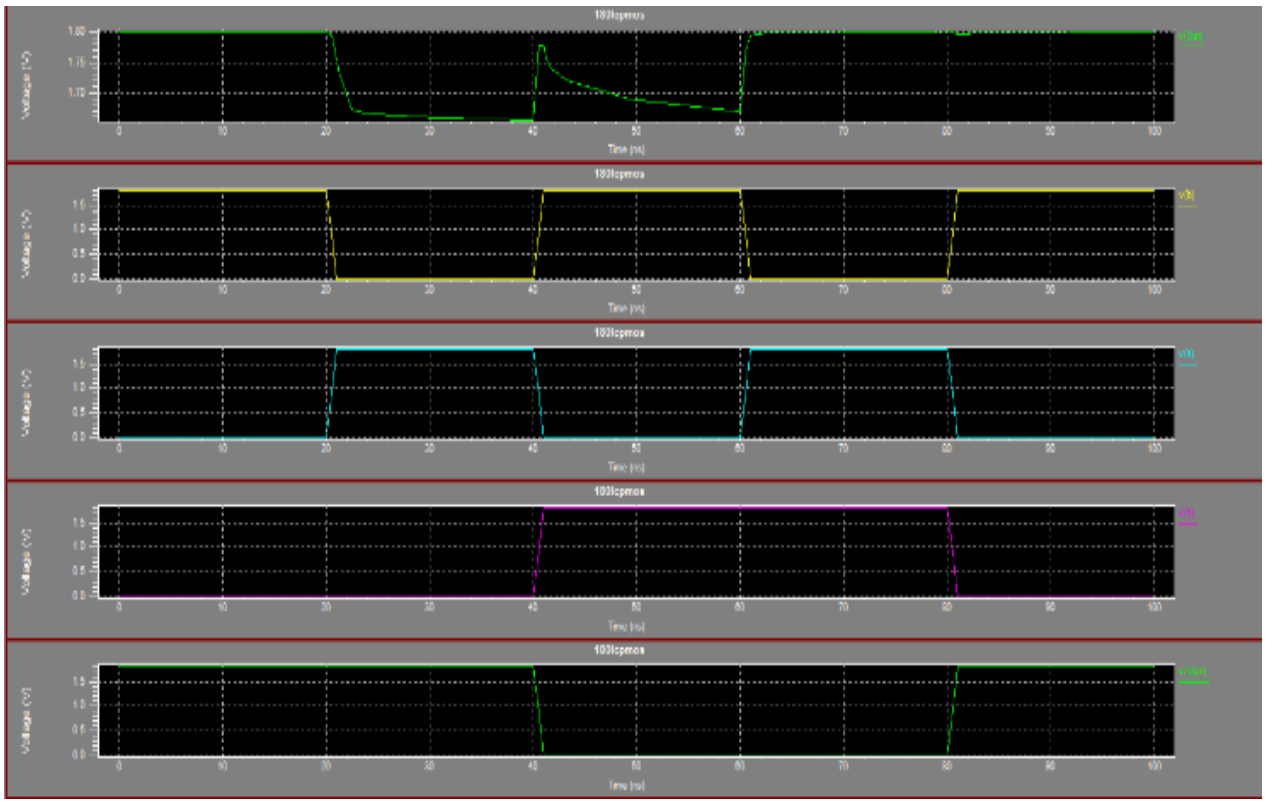

Figure 13: 2:1 Multiplexer output waveform for 180nm

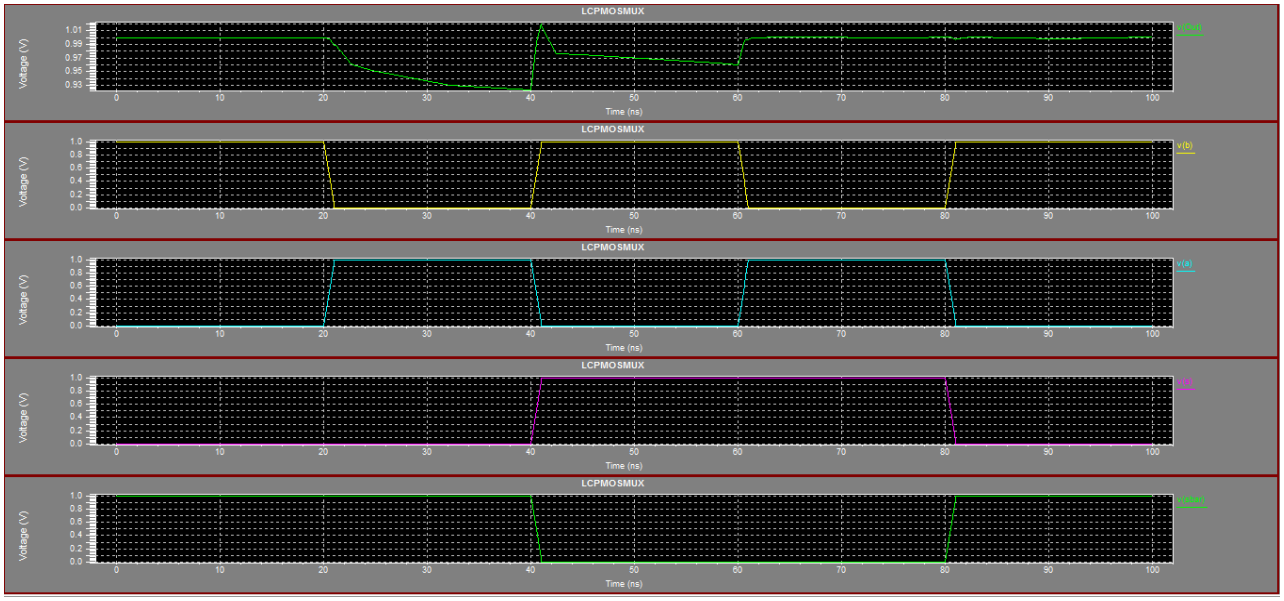

Figure 14: 2:1 Multiplexer output waveform for 90nm

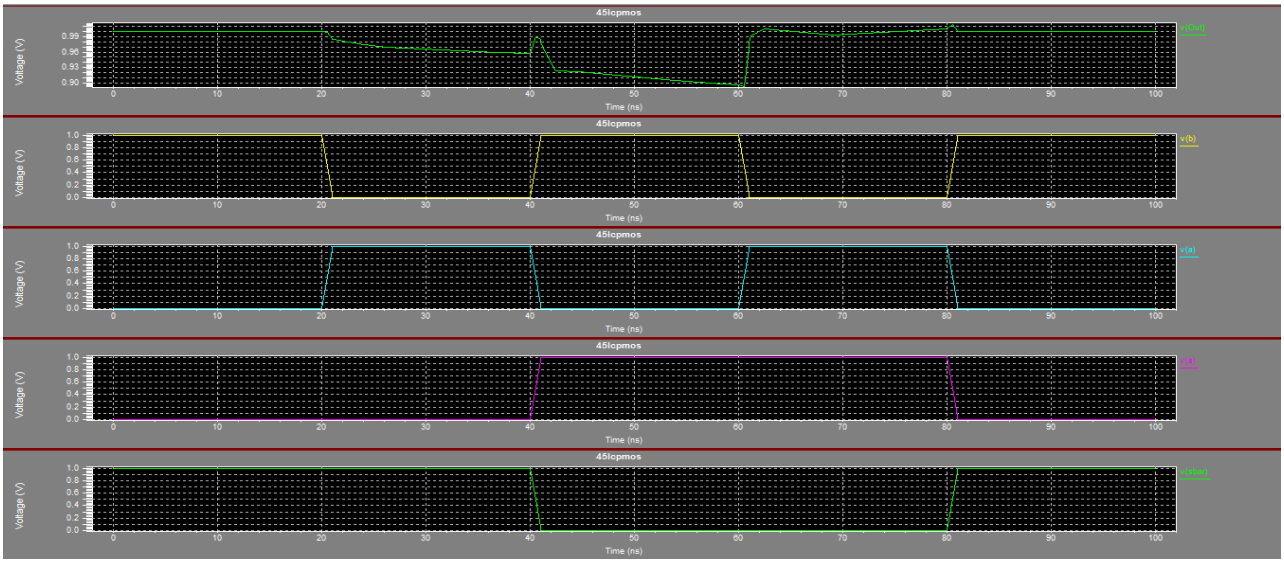

Figure 15: 2:1 Multiplexer output waveform for 45nm

C. Lector Technique

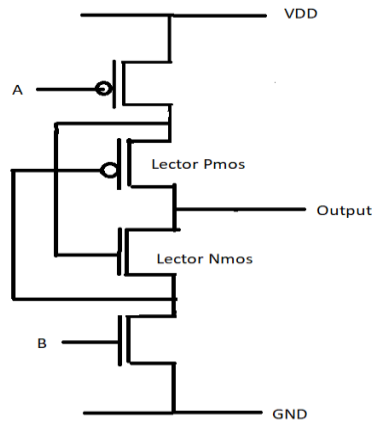

Figure 16: CMOS inverter using Lector

In this technique during standby mode, threshold voltage is elevated to a higher value by making substrate voltage either higher than supply voltage (for PMOS) or lower than ground (for NMOS)[12]. Two leakage control Transistors (LCTs) were introduced to each of thermos gates. This is done by adding a PMOS transistor to the Pull up network and a NMOS transistor to the pull-down network. The gate terminal of one the LCT is regulated by the source terminal of the other and any one of the LCTs will be in OFF state for any input given to the CMOS gate, by this an extra resistance will be formed in-between the path (from supply to ground). This decreases the sub-threshold leakage current and there by the static power is reduced.

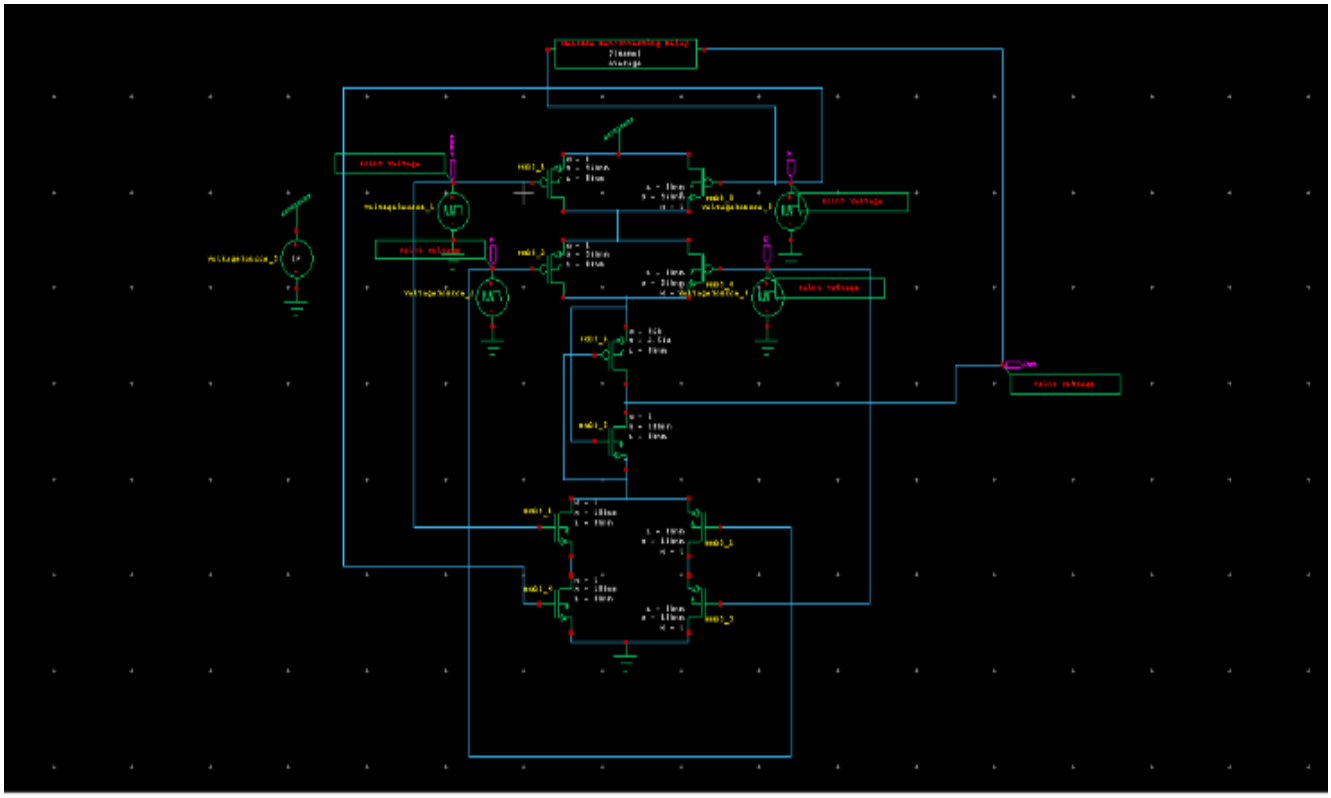

Figure 17: 2:1 multiplexer using Lector technique

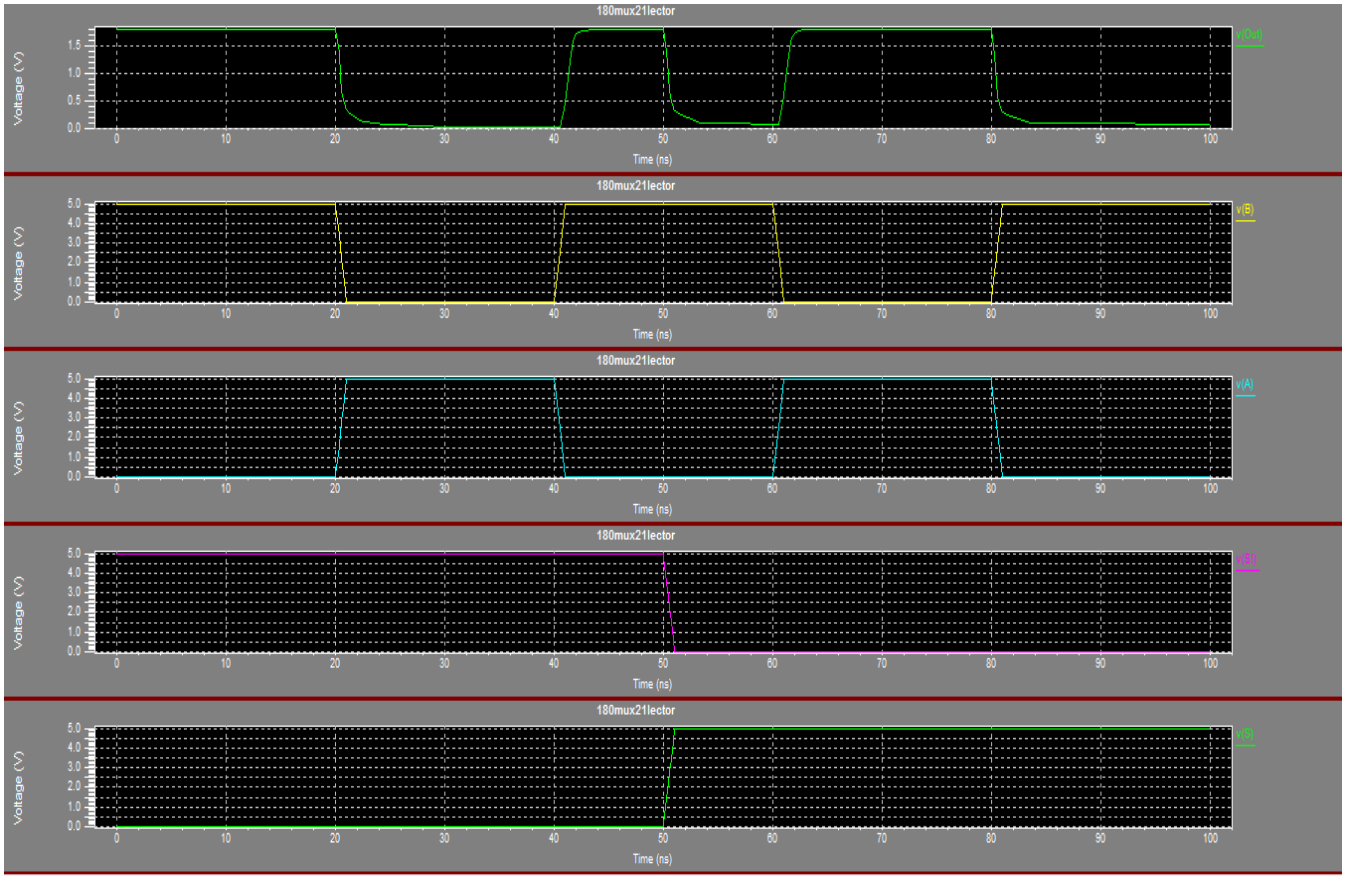

Figure 18: 2:1 Multiplexer output waveform for 180nm

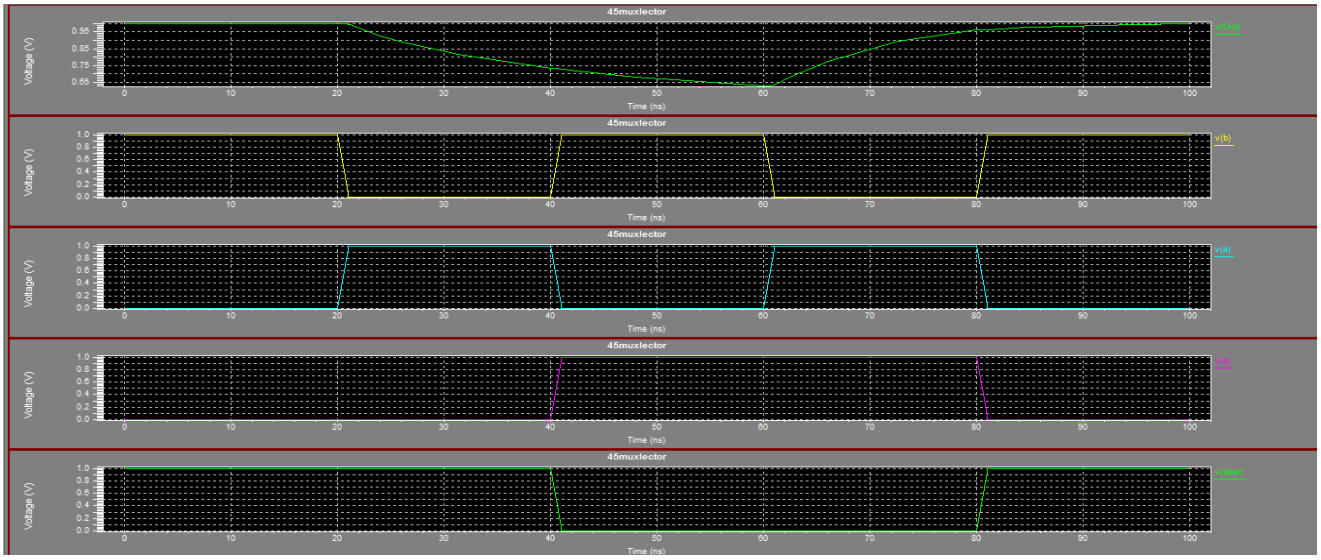

Figure 19: 2:1 Multiplexer output waveform for 90nm

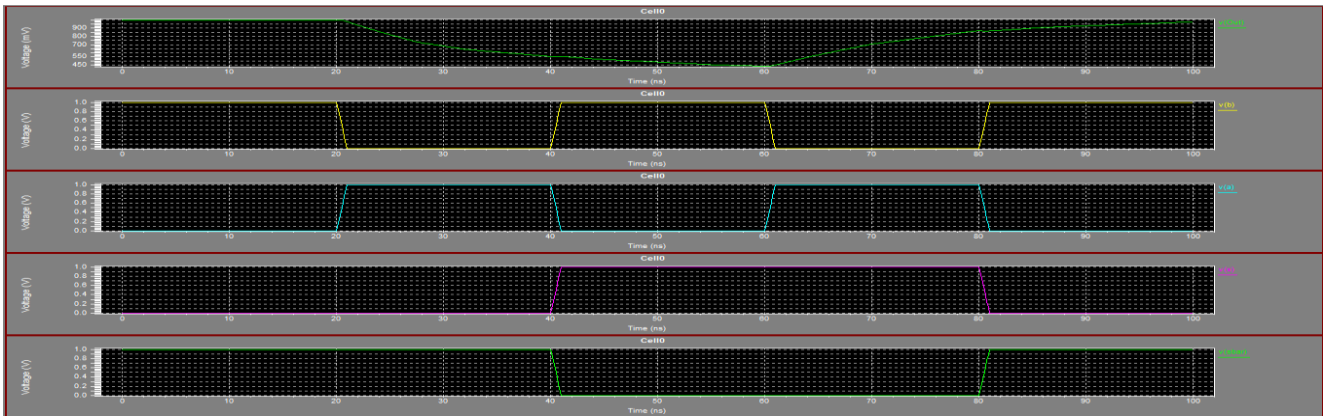

Figure 20: 2:1 Multiplexer output waveform for 45nm

Table 2: Comparison of different power reduction techniques with different nanometer technologies

Technique	180nm	90nm	45nm
CMOS	3.007123e-006W	3.75683e-007W	2.520625e-007W
LCnmos	1.871549e-006W	3.928740e-007W	2.715874e-009W
LCpmos	3.373305e-007W	9.163672e-009W	7.85727e-009W
LECTOR	3.786099e-009W	9.95141e-006W	3.192832e-006W

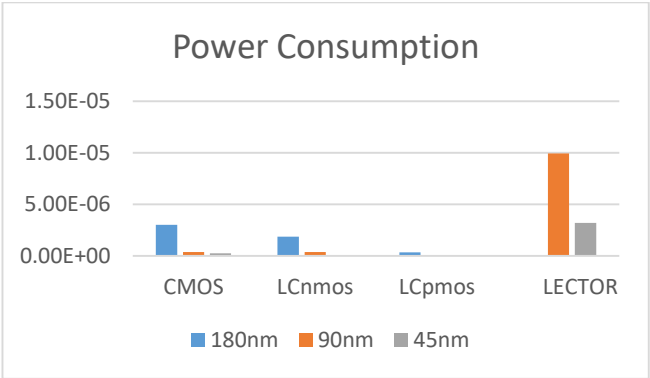

Figure 21: Comparison of power reduction techniques

IV. CONCLUSION

The leakage power consumption is a great challenge in nano-meter scale (CMOS) technology, although previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, based upon technology & design criteria the designers can choose the techniques. In this paper we provided few power consumption techniques that can be used for the designing of VLSI circuits. From all the mentioned power reduction techniques, LCpmos technique has very low power consumption with a power

consumption value of $7.85727e^{-009}$W when compared to that of LCnmos and Lector techniques in 45nm technology. Therefore, a circuit can be designed using the LCpmos power reduction technique with 45 nm technology.

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