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Secure Car Parking System Using VHDL

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ABSTRACT- The usage of automobiles is rising nowadays days and people, resulting in more pollution, traffic jams, and parking space difficulties, with finding a free parking spot becoming increasingly challenging. A Verilog HDL-based system for safe automotive parking management is proposed in this research. This machine is made up of three main parts. To begin, locate the vacant slot and determine the distances. Second, book the appointment in online mode. The entering and exit of passwords are addressed. Safety measures number three. Our execution time is drastically reduced when we use FPGA. This project is about building a software that simplifies the process of finding available parking spots and monitoring of parked cars in a parking lot. Due to the huge increase in availability and utilisation of parking spaces, finding an empty spot has become significantly more difficult. In recent years, there has been an increase in the number of automobiles. As the number of automobiles on the road grows, traffic congestion and pollutants increase (noise and air pollution). An FPGA-based parking system has been developed to overcome this issue. This article uses terminology like empty parking, Verilog HDL, traffic congestion, and vehicles.

KEYWORDS- VHDL, Xilinx, sensor, VHDL, proximity sensor.

I. INTRODUCTION

In this realistic setting, each individual did multiple jobs without fail. As a result, sensible efforts should be taken to prevent time loss in inefficient areas, such as unproductive car parking, which is the most regularly utilised activity, in order to complete all processes for the most effective utilization of resources. As a consequence, this research presents a way for making the best use of time when parking, which itself is connected to the security problem. The most significant subject outlines the following tactics for making the best use of time while also providing a safe park free of hazards. The main goal is to develop a parking system that is both secure and efficient. The usage of a password when parking, as well as the presentation of the passcode, is required for security. The total number of openings concentrated in a single slot, as well as the distance to barriers, are all calculated using the number of available vacancies and their locations (only adjacent vacancies are necessary). For public services, a parking facility is necessary. that might work in harmony with other government services

The total number of openings concentrated in a single slot, as well as the distance to barriers, are all calculated using the list of available vacancies and their locations (only adjacent vacancies are necessary). A parking system is designed for public services to function correctly and in concert with other reprogrammable public utilities. It is simple to update the FPGA-based design by changing the software component. Our service is designed for FPGA design and gate level simulation.

II. LITERATURE SURVEY

The suggested work has been the subject of a number of studies. [2] demonstrates that the method is feasible. This technique is cost-effective and incorporates a number of smart parking management features. The main goal of the project is to eliminate problems that we encounter in our daily lives when parking our automobiles.[1] Parking automobiles is becoming more and more of a challenge. In order to assure that this would not be repeated, a literature survey was conducted. This was made with MATLAB and relies on cameras to find available parking spaces. This application was used to assess parking lot occupancies by processing images taken by a surveillance camera in real time. A central control unit is used to process the data. The data is analysed by a central control unit before being sent to display panels strategically placed across the parking lot. The drivers will be able to see the vacant parking lot thanks to the details on the panels [3].

III. PROPOSED METHOD

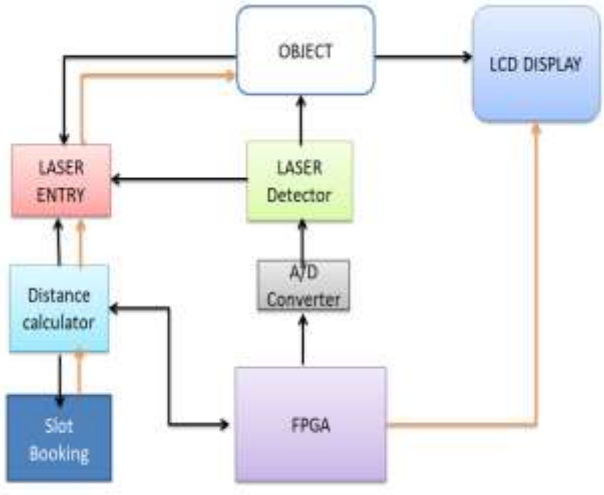

Figure 1: Block diagram of car parking system

There are three stages to the proposal. The target hardware in the first step is a Xilinx FPGA. The intended hardware in the second step is an application-specific integrated circuit (ASIC) using VHDL and standard cells. The FPGA framework's design process is further divided into three sections. The first stage is to create a software product, with the entire system written in C for the Xilinx MicroBlaze soft processor system. The second is a mixed hardware/software implementation, in which one half of the device is written in C and the other is written in hardware. The hardware is built using the words used to describe VHDL[4]. The third and final item .The hardware for the Xilinx XUP Virtex-IV Pro Development System will be finished and implemented.

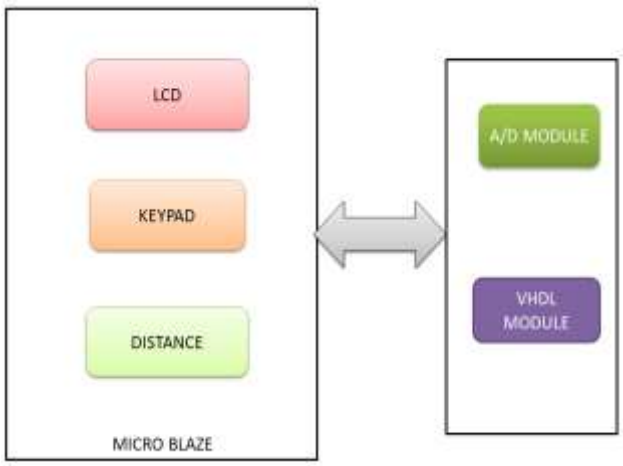

Figure 2: Block diagram of system

A test vector generator named "AD model" is created in VHDL to emulate the "Source" and "Echo" laser signal pulses.

In each measurement, 256 samples should be used. Finally, the device should be capable of calculating velocity and simulating movement. The optical filter, which has five taps for correlation, is the second block.

Both the reference and echo signals must be divided to calculate the interpolation. The division is handled by a distinct block that designs quick, non-restoring division. Because division cannot handle negative numbers, it is necessary to check the value sign, fig. [1] Show the schematic diagram analysis for the digital entry, how the connect the logic gates as high and low between gates. The fig 2 shows the block diagram of the distance measurement for the car parking slot through the distance calculation. To do a two-complement and then use the division result to calculate j correctly. This is repeated two more times until both echo and jerk have been determined. The first, as already said, is predetermined. The pre-calculated and implemented the speed of light and sampling frequency as a constant within the block, as we did in the previous computation. Design of Simulation in Xilinx ISA shows that Result analysis fig [3]. It shows the time delay between gates and logical analysis for the speed of the gates and difference time delay and power consumptions also showing the analysis for the synthesis report. Fig [4] shows that simulation analysis for the VLSI ise for the simulation results fig [5]. The results shows that when car entered the in parking area led will be high and when slot aloes booked they show in as high when parking is closed to led will be low .its showing as simulation Result as simulation Design Process. Fig [6]. It can also provide environmentally friendly help for halting the board. As a result, total greenhouse gas emissions will be lower, and the ecosystem will be cleaner.

IV. RESULT ANALYSIS

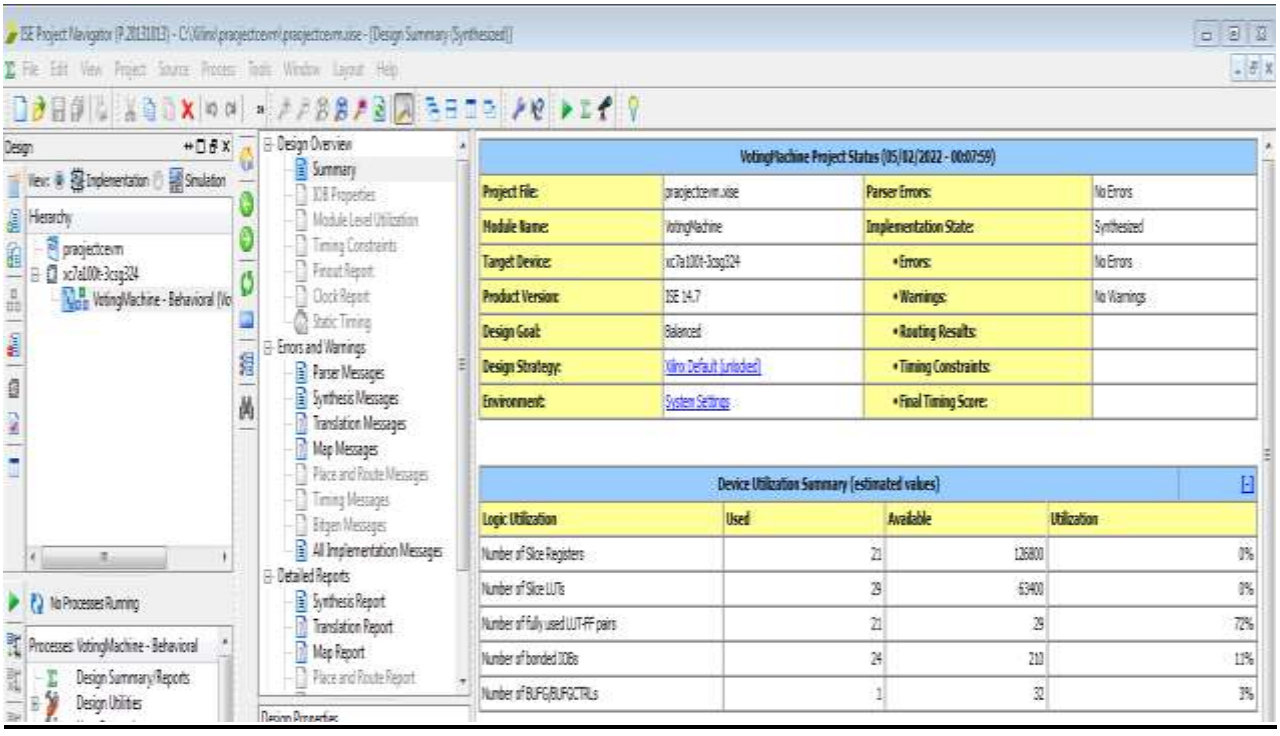

Figure 3: Device usage details

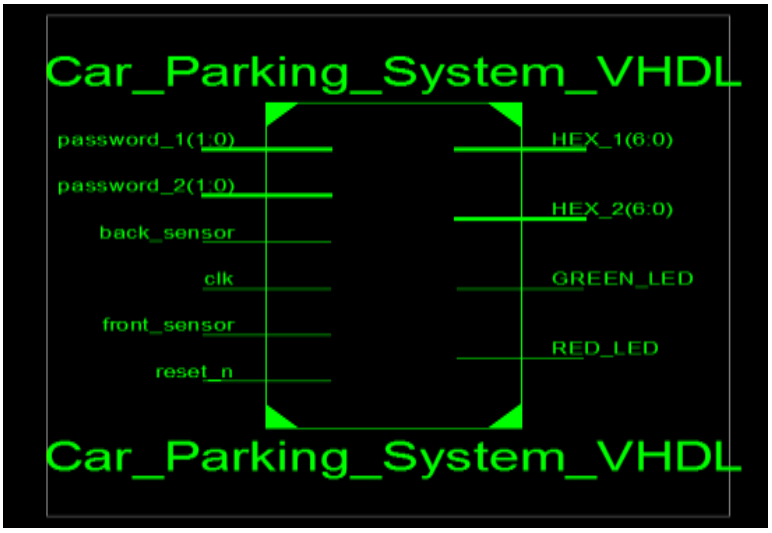

Figure 4: Block Diagram of Car parking System

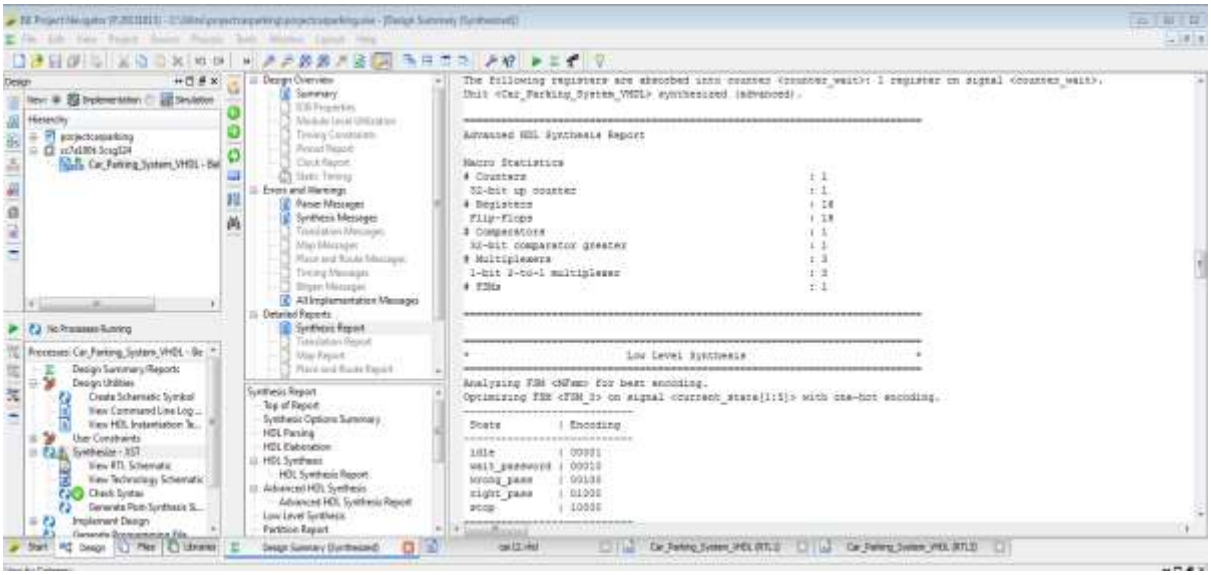

Figure 5: Synthesis Report

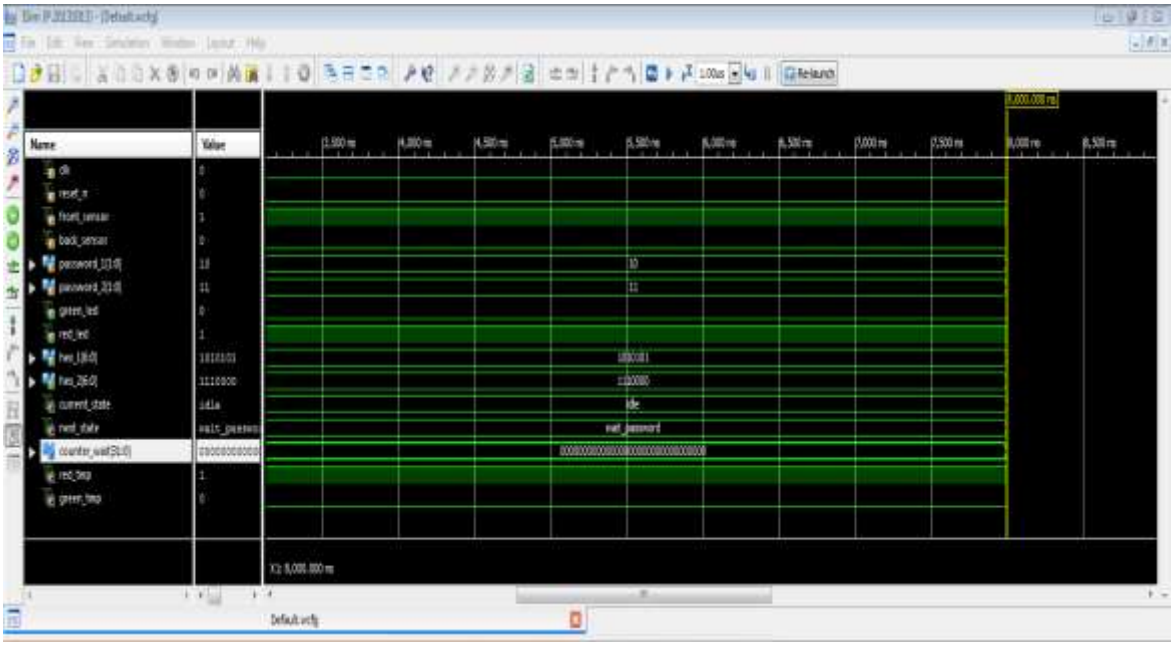

Figure 6: Simulations Result

V. CONCLUSION

The Proposed design of secure parking system is Enhancing with xilinx 14.7 the design is guaranteed in the Virtex 7 FPGA kit. Government equipment is increasing productivity, reduces costs, and speeds up marketing time. FPGA-based parking system, provides quick response. The key benefits are saved time and reduced traffic congestion. It can also provide environmentally friendly help for halting the board. As a result, total greenhouse gas emissions will be lower, and the ecosystem will be cleaner. This framework has a lower support cost, which helps the building designer save money.The designed system can be used in many programs and can be easily upgraded slot selection number. Parking is easy with the Designed system.

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